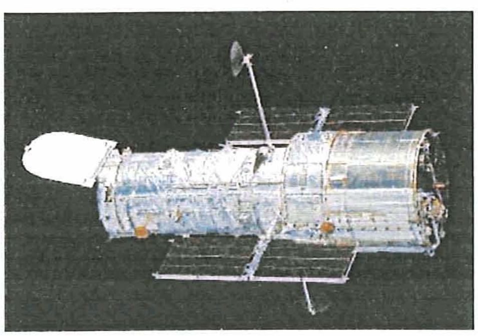
# Space Electronics
## A challenging world for designers

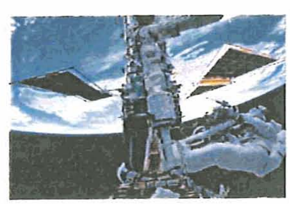
Christian Poivey
Kenneth A. LaBel
NASA-GSFC



## Designing Electronics for Space

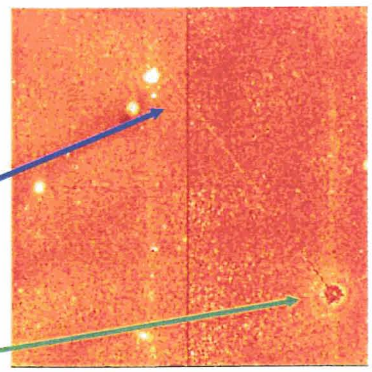



- •Low power
- •High reliability
- •Harsh environment
  - •Thermal
  - •Mechanical
  - •Electro-magnetic
  - •Radiation



# Outline

- The Space Radiation Environment
- The Effects on Electronics
- The Environment in Action
- Hardening Approaches to Commercial CMOS electronics
  - CMOS devices vulnerabilities
  - Hardening approaches
- Conclusion



Atomic Interactions
- Direct Ionization

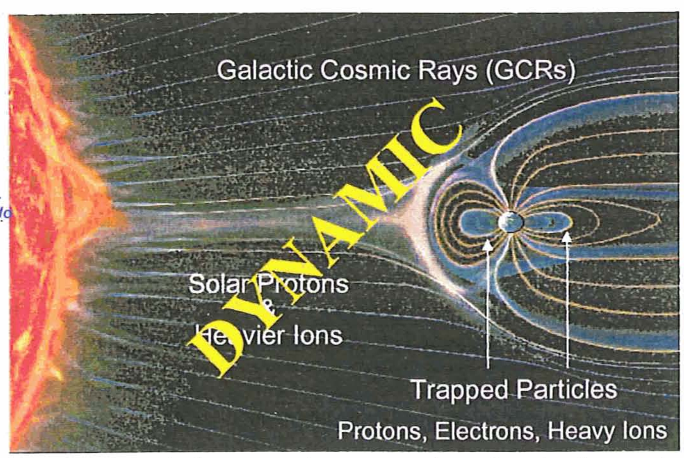
Interaction with Nucleus
- Indirect Ionization
- Nucleus is Displaced

*http://www.stsci.edu/hst/nicmos/performance/anomalies/bigcr.html*



# Space Radiation Environment

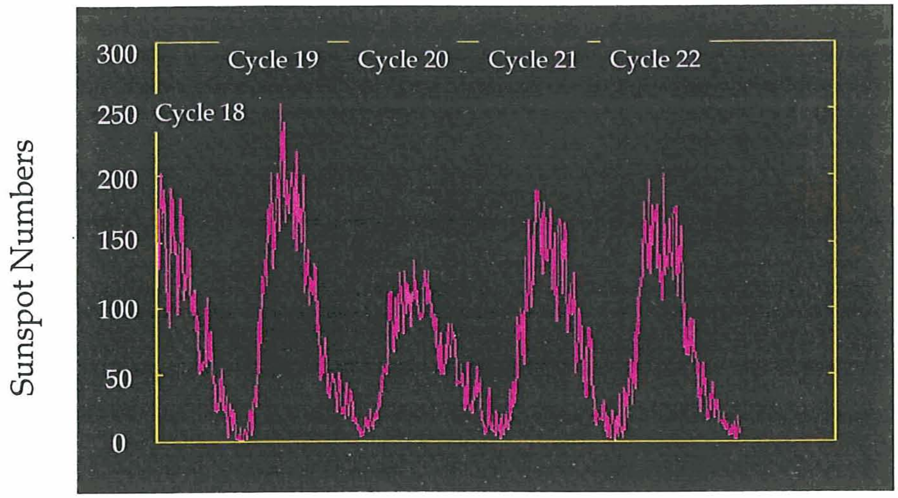
*Nikkei Science, Inc. of Japan, by K. Endo*




***Deep-space missions may also see: neutrons from background or radioisotope thermal generators (RTGs)***
***Atmosphere and terrestrial may see GCR and secondaries***

## Sunspot Cycle:
## An Indicator of the Solar Cycle

*after Lund Observatory*



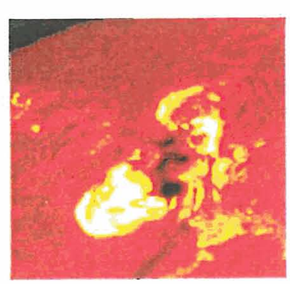

Length Varies from 9 - 13 Years
7 Years Solar Maximum, 4 Years Solar Minimum



## Solar Particle Events

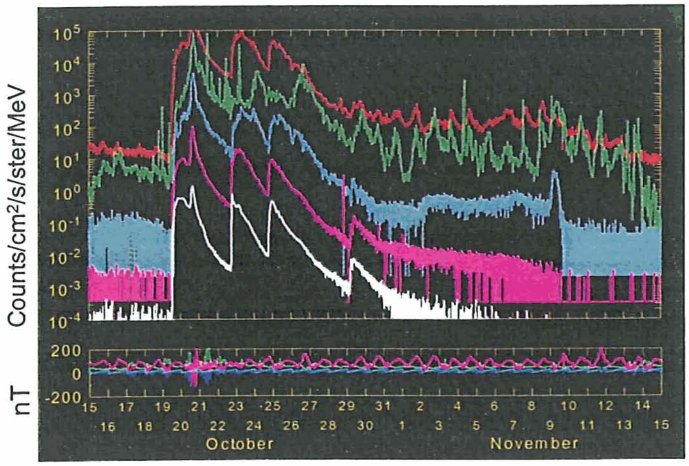
- Cyclical (Solar Max, Solar Min)
  - 11-year AVERAGE (9 to 13)
  - Solar Max is more active time period
- Two types of events
  - Gradual (Coronal Mass Ejections – CMEs)
    - Proton rich
  - Impulsive (Solar Flares)
    - Heavy ion rich
- Abundances Dependent on Radial Distance from Sun
- Particles are Partially Ionized
  - Greater Ability to Penetrate Magnetosphere than GCRs

*Holloman AFB/SOON*



## Solar Proton Event - October 1989

**Proton Fluxes - 99% Worst Case Event**



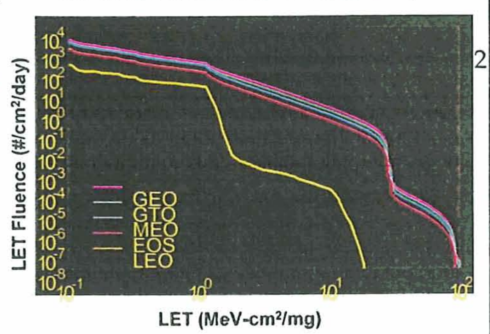

GOES Space Environment Monitor



## Free-Space Particles: Galactic Cosmic Rays (GCRs) or Heavy Ions

- Definition
  - A GCR ion is a charged particle (H, He, Fe, etc)
  - Typically found in free space (galactic cosmic rays or GCRs)
    - Energies range from MeV to GeVs for particles of concern for SEE
    - Origin is unknown
  - Important attribute for impact on electronics is how much energy is deposited by this particle as it passes through a semiconductor material. This is known as Linear Energy Transfer or LET (dE/dX).

**CREME 96, Solar Minimum, 100 mils (2.54 mm) Al**

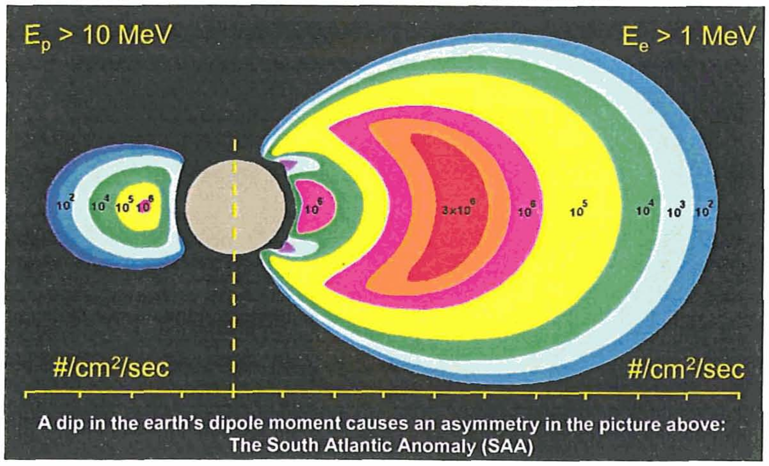



*Time*

*Commercial Technology Sensitivity*

## Trapped Particles in the Earth's Magnetic Field: Proton & Electron Intensities

AP-8 Model AE-8 Model

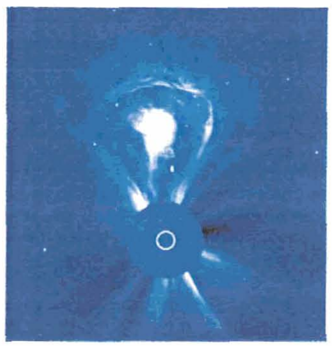



L-Shell



## Solar Cycle Effects: Modulator and Source

- Solar Maximum
  - Trapped Proton Levels Lower, Electrons Higher
  - GCR Levels *Lower*
  - Neutron Levels in the Atmosphere Are Lower
  - Solar Events More Frequent & Greater Intensity
  - Magnetic Storms More Frequent --> Can Increase Particle Levels in Belts
- Solar Minimum
  - Trapped Protons Higher, Electrons Lower
  - GCR Levels *Higher*
  - Neutron Levels in the Atmosphere Are Higher
  - Solar Events Are Rare



*Light bulb shaped CME courtesy of SOHO/LASCO C3 Instrument*

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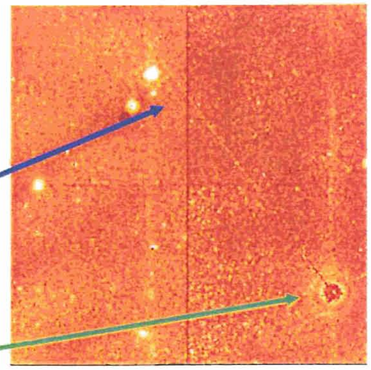

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# Radiation Effects and Spacecraft

- High energy particles loose energy when they cross electronic parts materials and cause radiation effects
  - Long-term effects
    - Total ionizing dose (TID)
    - Displacement damage
  - Transient or single particle effects (Single event effects or SEE)
    - Soft or hard errors

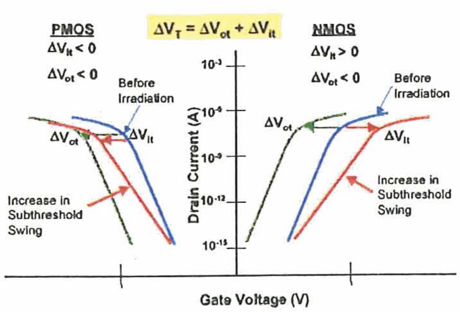
*An Active Pixel Sensor (APS) imager under irradiation with heavy ions at Texas A&M University Cyclotron*

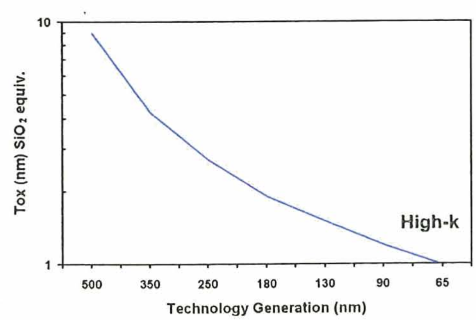
# Total Ionizing Dose (TID)

- **Cumulative long term *ionizing* damage due to protons & electrons**
  - Incident particles transfer energy to material through electron hole creation. Holes are trapped within devices' oxides or the interfaces oxide/silicon.
- **Effects**
  - Increase of Leakage Currents
  - Degradation of logical input levels and noise margin
  - Degradation of fan out
  - Degradation of propagation delays
  - Functional Failures
- **Unit of radiation: dose in Gray or rad**
  - 1 Gray = 100 rad = 0.01 J/Kg



# TID-induced threshold voltage shifts effects in CMOS devices



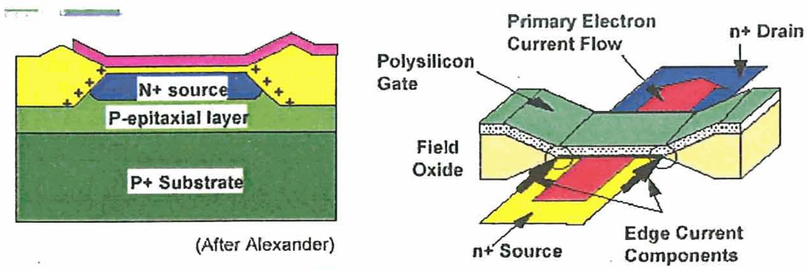



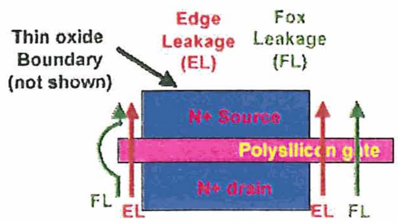

After Grove, IEDM02

$\Delta V_T \,\alpha\, t^2_{ox}$ (After Mc Garrity)

When $t_{ox} < 5$ nm, significant hole tunneling out of the gate oxide occurs, resulting in negligible number of remaining holes: $\Delta V_{ot} \sim \Delta V_{it} \sim 0$

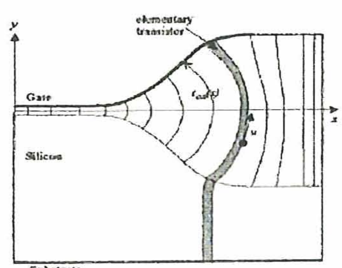
## TID-induced intra device edge leakage



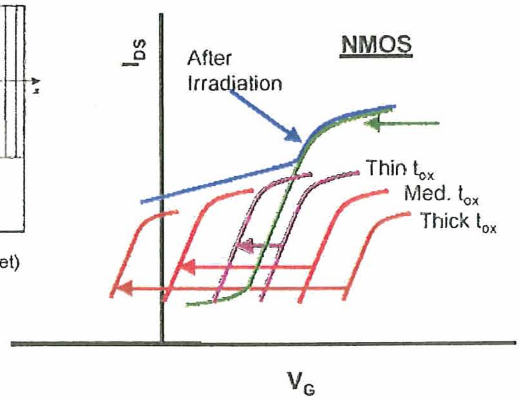





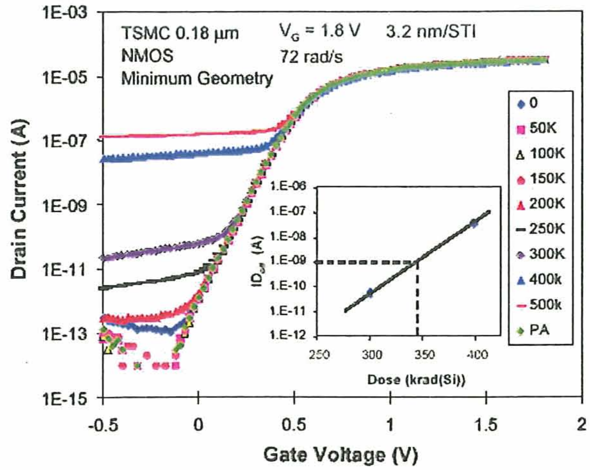

## Edge Leakage – Basic Mechanism




(After Brisset)



# Example of Edge Leakage for 0.36/0.18 µm NMOS Transistor

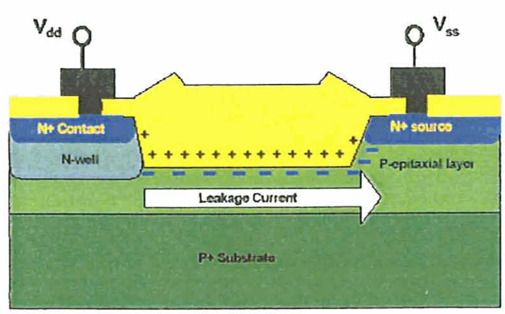



After Lacoe, EWRHE 2004



# Inter device isolation-oxide leakage

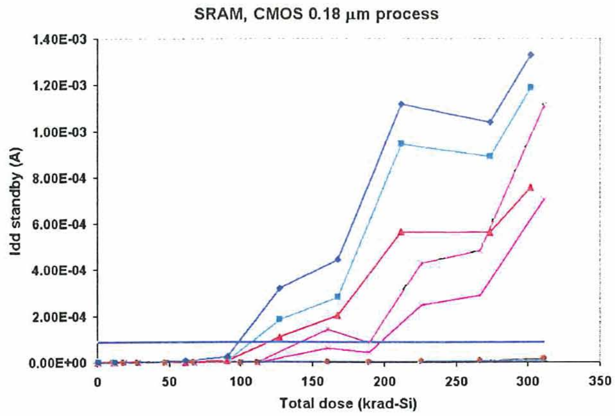
- Inversion of field oxide results in leakage path between N+ contact (Vdd) in the N- well and N+ source (GND)
- Field oxide leakage paths can also span N+ source/drain regions between adjacent N- channel transistors




*Field oxide leakage path*

(After Alexander)

## Example of TID degradation for 0.18 μm CMOS SRAM



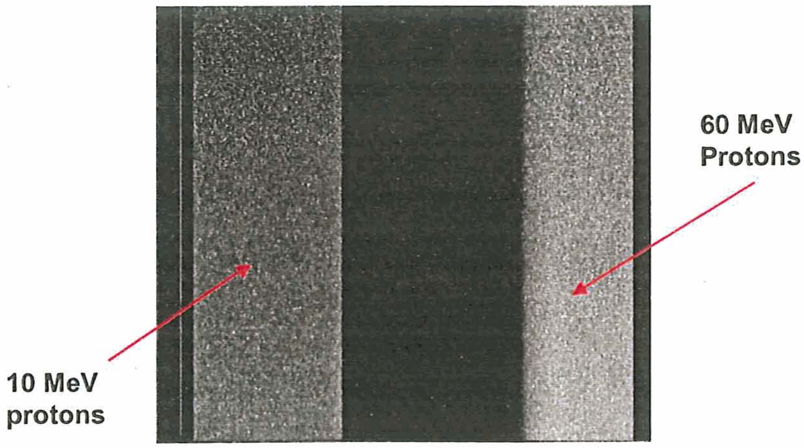

- No significant degradation up to 90 krad-Si
- Sufficient for most space applications, typical dose levels:
    - Geostationary Orbit, 10 years: 50 krad-Si
    - Low Earth Orbit, 5 years: 20 krad-Si



## Displacement Damage (DD)

- Cumulative long term *non-ionizing* damage due to protons, electrons, and neutrons
    - Incident particles transfer energy by elastic or inelastic collisions with atoms of the devices material (Silicon). Structural defects are created on the crystallographic structure.
- Effects
    - Minority carrier lifetime in the semiconductor is decreased
        - Increase leakage currents
        - Decrease gain of bipolar transistors
    - Important for opto-electronics and linear bipolar devices, not significant for CMOS devices.
- Unit of radiation:
    - equivalent fluence for a selected electron or proton energy in particles/cm$^2$

## DD damage example, CCD

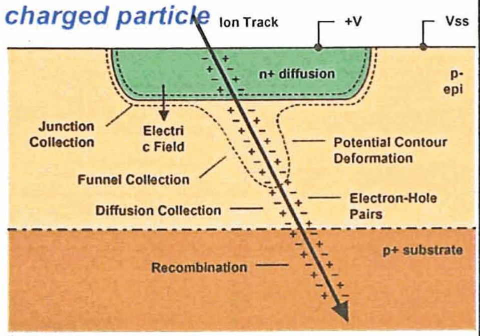



(After Hopkinson RADECS 03 short course)



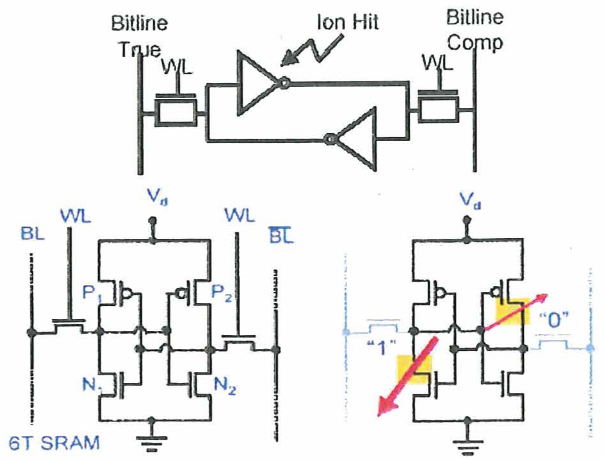
## Single Event Effects (SEEs)

- *Ionizing* effect caused by a *single charged particle*
  - Heavy ions
    - Direct ionization
      - Creation of a very dense plasma of electrons hole pairs
      - The pairs that do not recombine are separated by the junction electric field, and a current spike is generated.
  - Protons for sensitive devices
    - Nuclear reactions for standard devices
- Unit of radiation:
  - LET (Linear Energy Transfer) in MeVcm²/mg
- If the LET of the particle (or reaction) is greater than the amount of energy or critical charge required, an effect may be seen



# Single Event Upset (SEU)

When SEU current $I_{SEU}$ exceeds restoring current from cross-coupled inverter such that the node voltage drops below $V_D/2$ for too long, an upset occurs

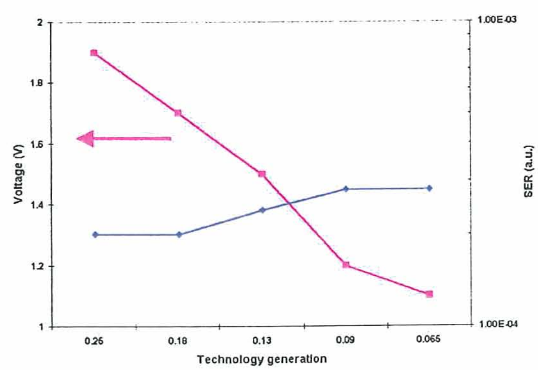



(After Baumann)



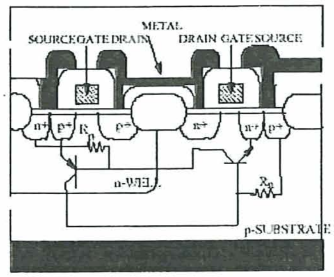
# SEU trend on SRAM

- At fixed voltage SER decreased by 13% per generation.
- At the nominal voltage for each generation (14% scaling per generation), the SER sensitivity has increased by about 8% per generation.



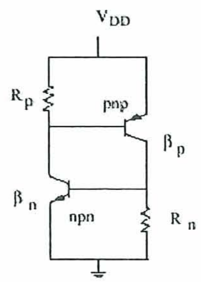

After Hazucha, IEDM 03

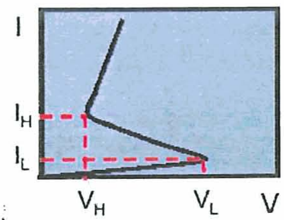
# Single Event Latchup (SEL) in CMOS circuits




Latchup can cause circuit lockup and/or catastrophic device failure

SCR



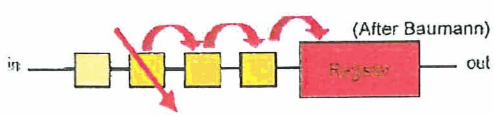

- If an energetic particle produces $I>I_L$, $\beta_n\beta_p>1$ and $V_{DD}>V_H$, then latchup will occur
- As technology scales, soon $V_{DD}<V_H$ and latchup is no longer a problem
- Epi reduces $R_n \Rightarrow$ increase latchup threshold

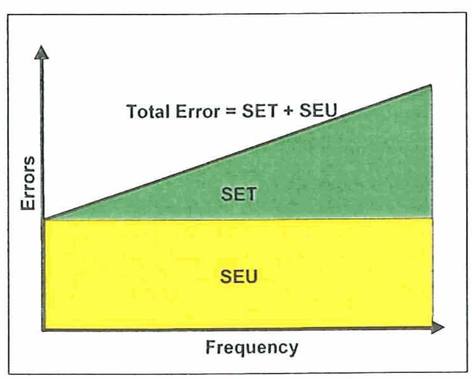


# Single Event Transient (SET)

- Voltage transients can propagate through combinatorial logic
  - Indistinguishable from normal signals
  - Incorrectly latched if arrive at clock edge
- Errors rates now depend on clock frequency
- Total error rate is the sum of the SEU + SET contributions

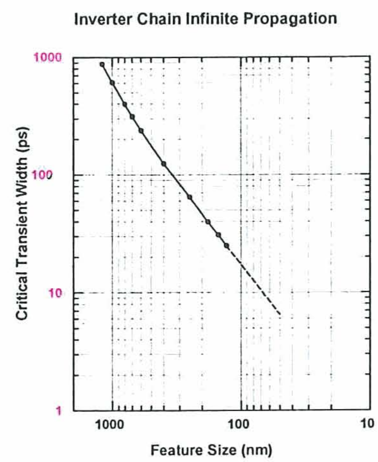
(After Baumann)



## Transient propagation in CMOS

- If transient pulse width is greater than critical width, the pulse will propagate indefinitely through combinatorial logic.
- For pulses shorter than the critical transient width, the transient will be attenuated.
- Critical width decreases with feature size
  - Estimate of heavy ion transient pulse width is 100-200 ps
  - SETs important for CMOS at or below 0.25 μm technology node



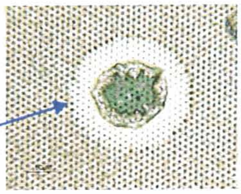

After Mavis, EWRH 04



## Other Single Event Effects

| | | |
|---|---|---|
| Multiple Event Upset (MEU) | Several bits corrupted by a single particle | Memories |
| Single Event Functional Interrupt (SEFI) | Loss of normal operation | Complex devices with built-in state machine/control sections |
| Single Event Burnout (SEB) | High current condition | BJT, N channel power MOSFETs |
| Single Hard Error (SHE) | Stuck bit | Memories |
| Single Event Gate Rupture (SEGR) | Rupture of gate dielectric | Power MOSFETS, flash PROM,... |
| Other events | SESB, HCA,.... | |

*Destructive event in a MOSFET used in a DC-DC Converter*



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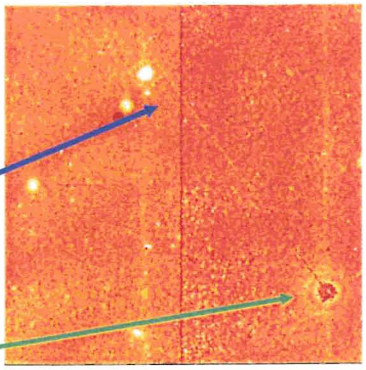

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*http://www.stsci.edu/hst/nicmos/performance/anomalies/bigcr.html*



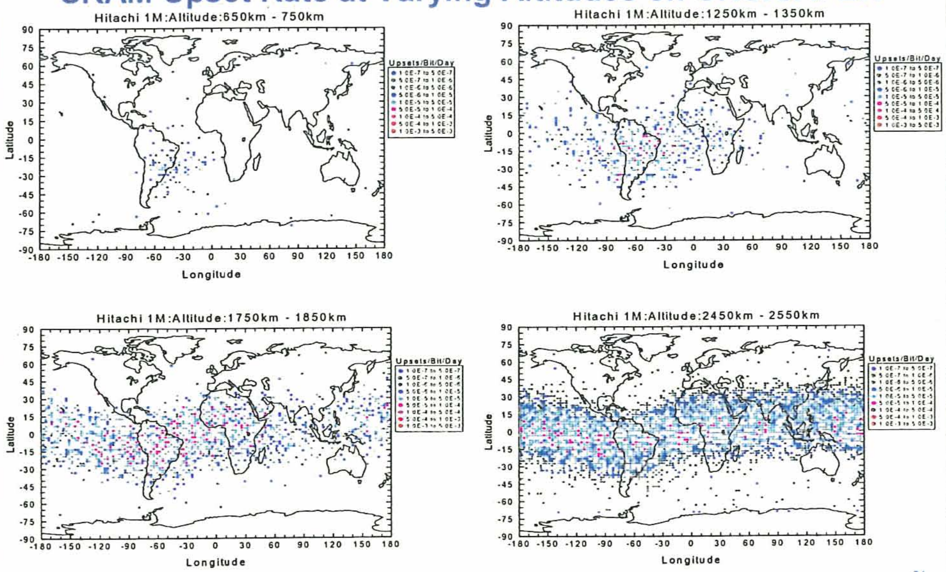
# Radiation Effects on Electronics and the Space Environment

- Three portions of the natural space environment contribute to the radiation hazard
  - Solar particles
    - Protons and heavier ions
      - SEE, TID, DD
  - Free-space particles
    - GCR
      - For earth-orbiting craft, the earth's magnetic field provides some protection for GCR
      - SEE
  - Trapped particles (in the belts)
    - Protons and electrons including the South Atlantic Anomaly (SAA)
      - SEE (Protons)
      - DD, TID (Protons, Electrons)

The sun acts as a modulator and source in the space environment

# SAA and Trapped Protons:

## Effects of the Asymmetry in the Proton Belts on SRAM Upset Rate at Varying Altitudes on CRUX/APEX




DCIS04 – Space Radiation Effects presented by Christian Poivey, Bordeaux, France, November 26, 2004

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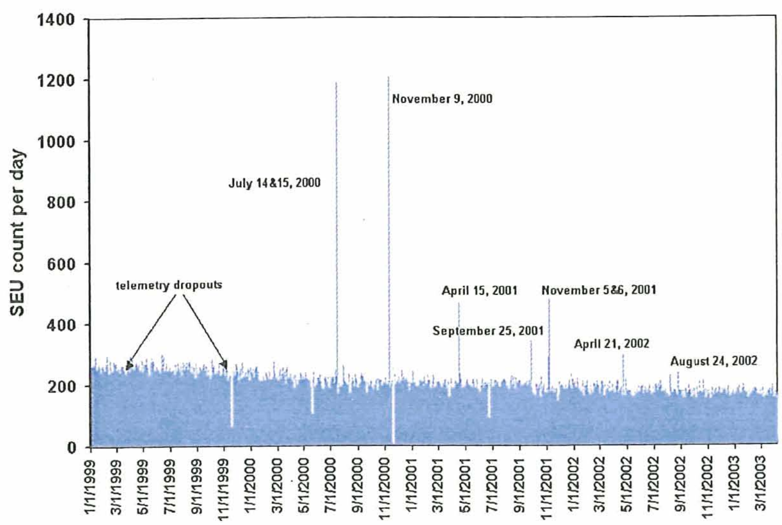
# Background environment and solar events

## SRAM upset rate versus time on Orbview-2 SSRs

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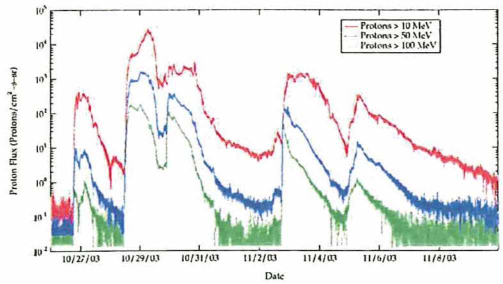
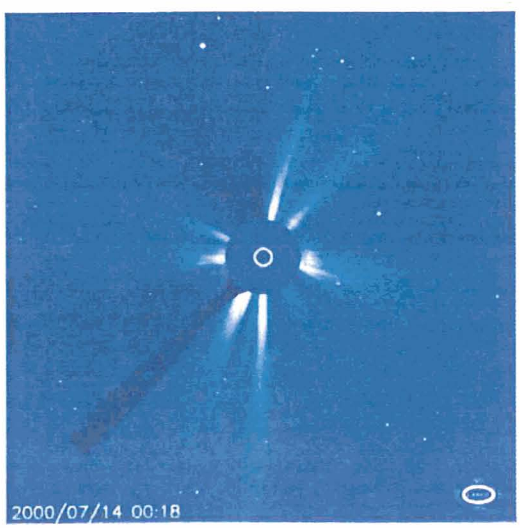
# Recent Solar Events – A Few Notes and Implications

- In Oct-Nov of this year, a series of X-class (X-45!) solar events took place
  - High particle fluxes were noted
  - Many spacecraft performed safing maneuvers
  - Many systems experienced higher than normal (but correctable) data error rates
  - Several spacecraft had anomalies causing spacecraft safing
  - Increased noise seen in many instruments
  - Drag and heating issues noted
  - Instrument FAILURES occurred
  - Two known spacecraft FAILURES occurred
- Power grid systems affected, communication systems affected...



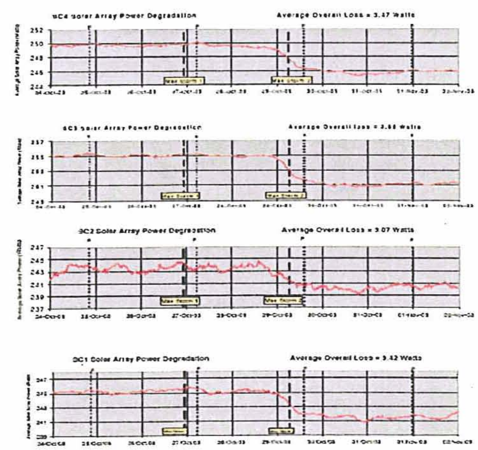



# SOHO LASCO C2 of the Solar Event



## Solar Event Effect - Solar Array Degradation on CLUSTER Spacecraft

ANNEX 1: Evolution of the Solar Array Power from 24-Oct to 02-Nov 2003 when two solar radiation storms occurred (the time of their maximum is indicated in the plot "---")
The degradation of the panels was about 1.4% and the average power loss is shown for each spacecraft.
The perigee passes are marked as "....." and labeled with "P"




Many other spacecraft to noted degradation as well.



## Science Spacecraft Anomalies During Recent Solar Events

| Type of Event | Spacecraft/ Instrument | Notes |
|---|---|---|
| Spontaneous Processor Resets | RHESSI | 3 events; all recoverable |
| | CLUSTER | Seen on some of 4 spacecraft; recoverable |
| | ChipSAT | S/C tumbled and required ground command to correct |
| High Bit Error Rates | GOES 9,10 | |
| Magnetic Torquers Disabled | GOES 9, 10, 12 | |
| Star Tracker Errors | MER | Excessive event counts |
| | MAP | Star Tracker Reset occurred |
| Read Errors | Stardust | Entered safe mode; recovered |
| Failure? | Midori-2 | |
| Memory Errors | GENESIS | 19 errors on 10/29 |
| | Many | Increase in correctable error rates on solid-state recorders noted in many spacecraft |

## Science Instrument Anomalies During Recent Solar Events

| Type of Event | Spacecraft/ Instrument | Notes |
|---|---|---|
| Instrument Failure | GOES-8 XRS | Under investigation as to cause |
| | Mars Odyssey/Marie | Under investigation as to cause; power consumption increase noted; S/C also had a safehold event – memory errors |
| | NOAA-17/AMSU-A1 | Lost scanner; under investigation |
| Excessive Count Rates | ACE, WIND | Plasma observations lost |
| | GALEX UV Detectors | Excess charge – turned off high voltages; Also Upset noted in instrument |
| | ACE | Solar Proton Detector saturated |
| Upset | Integral | Entered Safe mode |
| | POLAR/TIDE | Instrument reset spontaneously |
| Hot Pixels | SIRTF/IRAC | Increase in hot pixels on IR arrays; Proton heating also noted |
| Safe Mode | Many | Many instruments were placed in Safe mode prior to or during the solar events for protection |



## Selected Other Consequences

- Orbits affected on several spacecraft
- Power system failure
  - Malmo, Sweden
- High Current in power transmission lines
  - Wisconsin and New York
- Communication noise increase
- FAA issued a radiation dose alert for planes flying over 25,000 ft

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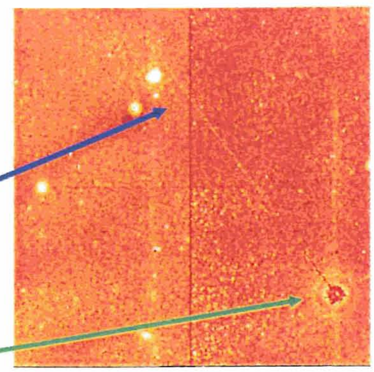

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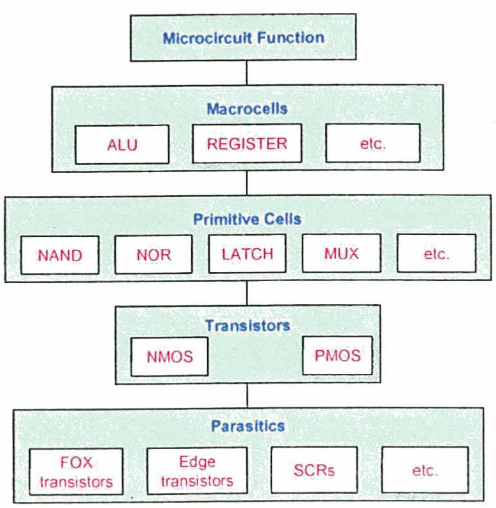
# Hardening by design to radiation effects




Layout:
Guard band/Guard ring
Spacing
Body ties

*Alexander, NSREC 96 short course*

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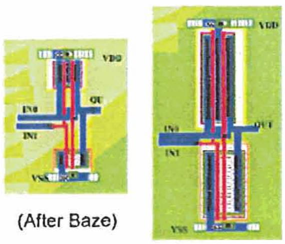
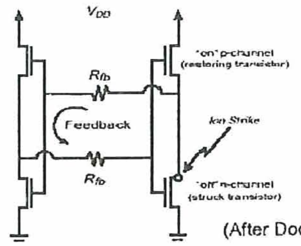
# SEU hardening at primitive cell level

Increased Drive Current



(After Baze)

Resistive Coupling




(After Dodd)

- •Increase Drive current $I_D$ (↑W) increasing restoring current
- •No speed penalty
- •Area penalty α $I_D$

- •Decrease response tine by increasing RC with feedback resistors
  - •Resistors are not an option at many commercial foundries
- •Speed penalty
- •Small area penalty

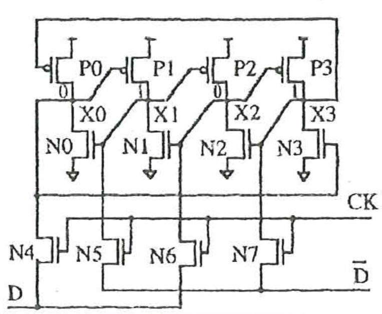


# SEU hardening at macrocell level

- Design enhancements: deal with SEU occurring in primitive cells
  - – Hardened data latches: DICE, HIT,..

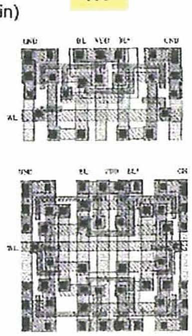
- • Uses a 4-node redundant structure
  - •Stores data as 1010 or 0101
- •Relies on dual node feedback control
  - • Two nodes must be struck simultaneously to generate an upset
- •Decrease in effective sensitive area

(After Calin)




DICE Circuit

1x

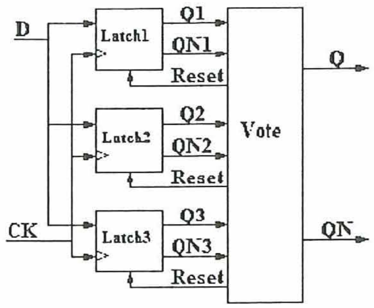


1.9x

## SEU hardening at macrocell level

- **Design enhancements: deal with SEU occurring in primitive cells**
  - **redundancies**

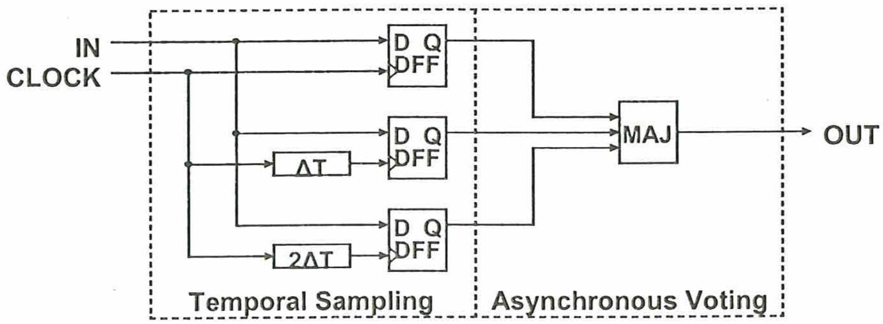
•Triple Module Redundancy (TMR)
Triple logic + vote
•Reduce effective sensitivity
•2 latches must be struck simultaneously to get an error
•Does not increase tolerance of individual latches
•~ 3x-4x power/area




(After Black)

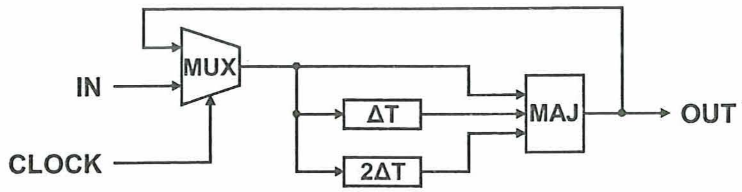


## SEU/SET hardening at macrocell level




• By delaying clocks, transient can only be captured at 1 latch
•Voted out
• Can delay data instead of clocks
•Sensitive to transients on clock line
•Area penalty ~ 3x – 4x
•Speed penalty: $1/f_{eff} = 1/f_0 + 2\,\Delta T$
•Many variations on this concept

## SEU/SET hardening at macrocell level

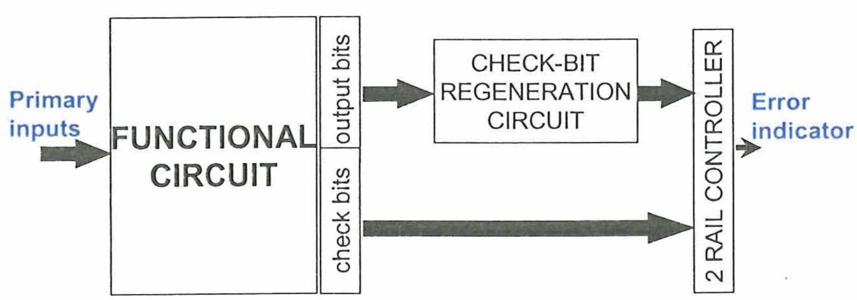



- Achieves equivalent of triple spatial redundancy by using same circuitry at three different times
- With appropriate ΔT, can be immune to upset from multiple node strikes
- Immune to transients on: data, clock, asynchronous control, and synchronous lines



## Hardening at the function level

- Design enhancement to deal with errors occurring in macrocells
  - Redundancies and voting or lockstep
  - EDAC/Self checking



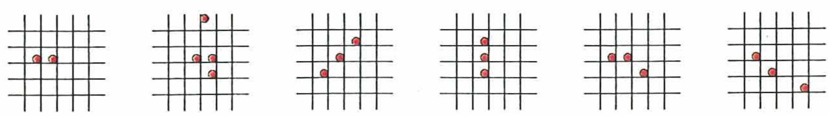

  - Watchdog timer

## EDAC example: Hamming code

- Parity evaluation of different bit combinations allows for m bit correct, n bit detection
- Can be used to correct/detect memory output
- Can be used to scrub memories
  - Time between scrubs determines max error latency

| Data Bits | Check Bits | Total bits |
|---|---|---|
| 1 | 3 | 4 |
| 2 to 4 | 4 | 6 to 8 |
| 5 to 11 | 5 | 10 to 16 |
| 12 to 26 | 6 | 18 to 32 |
| 27 to 32 | 7 | 34 to 39 |

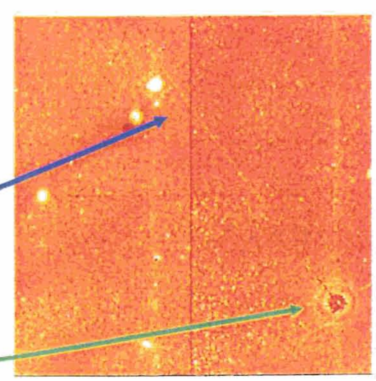
**Single Bit-Error Correct, Double Bit-Error Detect**





## Outline

- The Space Radiation Environment
- The Effects on Electronics
- The Environment in Action
- Hardening Approaches to Commercial CMOS electronics
  - CMOS devices vulnerabilities
  - Hardening approaches
- **Conclusion**



Atomic Interactions
- Direct Ionization

Interaction with Nucleus
- Indirect Ionization
- Nucleus is Displaced

*http://www.stsci.edu/hst/nicmos/performance/anomalies/bigcr.html*

## Conclusion

- The radiation environment makes the design of electronics for space very challenging
- High total dose hardness levels can be achieved with state of the art technologies
- A variety of design techniques exist for mitigating SEE
  - Area, power, speed penalties depend on chosen mitigation approach
- New effects occur for each new technology generation