Alternative Test Methods for Electronic Parts

For the NASA Electronic Parts and Packaging (NEPP) Program, 2004
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Introduction

It is common practice within NASA to test electronic parts at the manufacturing lot level to demonstrate, statistically, that parts from the lot tested will not fail in service using generic application conditions. The test methods and the generic application conditions used have been developed over the years through cooperation between NASA, DoD, and industry in order to establish a common set of standard practices. These common practices, found in MIL-STD-883, MIL-STD-750, military part specifications, EEE-INST-002, and other guidelines are preferred because they are considered to be effective and repeatable and their results are usually straightforward to interpret. These practices can sometimes be unavailable to some NASA projects due to special application conditions that must be addressed, such as schedule constraints, cost constraints, logistical constraints, or advances in the technology that make the historical standards an inappropriate choice for establishing part performance and reliability. Alternate methods have begun to emerge and to be used by NASA programs to test parts individually or as part of a system, especially when standard lot tests cannot be applied. Four alternate screening methods will be discussed in this paper: Highly accelerated life test (HALT), forward voltage drop tests for evaluating wire-bond integrity, burn-in options during or after highly accelerated stress test (HAST), and board-level qualification.

HALT

HALT first emerged when manufacturers started using it to force prototypes or pre-production units to failure in order to learn about particular failure modes and device design margins. Test conditions for HALT were determined based on the test item and its vulnerabilities with respect to its geometry, construction, or intended application. The term "acceleration" in the name, not originally intended to be used in the context of statistical reliability terms, refers to the highly elevated stress level used (usually temperature) to shorten the test time. HALT typically employs a combination of stepped temperature stress, rapid temperature transition, and vibration, where the test is continued until the component fails. Test durations are in the 50- to 100-hour range rather than in the 1,000- to 2,000-hour range used for reliability testing (life test). The vibration condition is the most effective for accelerating the effects of field life. The next most effective test is vibration performed simultaneously with rapid temperature stress.[1] The emphasis of HALT is stimulating the part to fail rather than simulating wear-out mechanisms.[2]

The failures typically found with HALT are broken leads, broken solder joints, broken traces, tolerance failures, shorts, and circuit design issues.[3] The operating limit is defined as the point at which the unit stops operating but returns to operation when the stress level is decreased. The destruct limit is the level at which the product stops functioning

and remains inoperable.[4] There is reluctance to standardize the way HALT is applied because it should be used to examine a particular design to draw out the primary failure modes or examine particular areas of interest, such as unsupported mechanical features in a vibration environment.[5]

The cost and time associated with establishing a failure rate for new or re-designed components has been found by many high-reliability programs to be difficult or impossible to absorb, so NASA and the DoD agencies are continually investigating new ways to establish the reliability of electronic parts and assemblies in ways that are faster and less costly. HALT was not established on the basis of providing an acceleration factor that will enable shortened life testing, achieving the same information about failure rate as traditional statistically based methods,[1] though there is continued interest in finding a way to make that correlation. Papers have been published in this spirit showing varying results.

Reference [6] reports HALT and traditional life-test results for multilayer ceramic capacitors from lots that had field failures. HALT conditions were 50% of the dielectric breakdown voltage (400 V, or eight times the rated voltage) and 140 ºC, and the standard test conditions were 100 V and 125 ºC. These HALT conditions represent a cubic voltage acceleration factor and an order of magnitude reduction in mean time to failure (MTTF) from the 15 ºC increase in test temperature over that used in the standard test. Calculated failure rates for the test groups (HALT vs. standard) showed relatively similar failure rates. Several failure modes were cited.

Reference [7] reports testing of copper interconnect test structures (trace and via combinations) in temperatures between 300 ºC and 460 ºC. The results indicated two separate failure mechanisms, one dominating at the lower test temperature and the other only appearing at the higher temperature. The assumption was that the very highly elevated temperature was producing conditions that were allowing significant changes to the structure of the interconnect material, a condition that would probably not be encountered in actual use regardless of the service life of the device. Conversely, recent investigations of bond-wire failures in laser diodes used by NASA found that the accelerated life testing done on the diodes, via accumulating millions of "shots" in a relatively short amount of time, did not provide the duration at temperature needed to grow the intermetallic material, which eventually caused them to fail.

Two recent test programs designed by NASA GSFC engineers have used HALT to examine multilayer ceramic capacitor (MLCC) lot viability. The first was focused on the failure modes and reliability of commercial off-the-shelf (COTS) vs. military-grade medium- to low-voltage MLCCs. The second was used to provide early-stage selection criteria for lots that would be submitted for full flight screening and qualification testing. The second test program was also used to discover if MTTF values could be extracted using the HALT results.

The first test program, reported through the Capacitor and Resistor Technology Symposium (CARTS) of 2004 by Michael Sampson and Jay Brusse,[8] involved 17

manufacturing lots of size 0805 and 0402 MLCCs with voltage ratings between 6.3 V and 50 V. Several sample tests were used as "reliability indicators": Voltage conditioning, HALT, destructive physical analysis (DPA), and ultimate voltage breakdown strength (UVBS). The voltage conditioning test was done using the standard military test method conditions. For HALT, the test voltage used was 6x rated voltage for parts rated below 50 V and 8x rated voltage for the 50 V rated parts. The DPA methods used were per the EIA RS-469 standard (one plane of cross-section only). The voltage breakdown strength test used voltage ramping until destruction at a rate of 10 V/sec. The results for the voltage breakdown strength test were normalized using ratios of the voltage breakdown strength versus the dielectric thickness. The results of these tests were compared to the results of traditional life tests done on the same lots to see if the any of the reliability indicator tests caused defective parts to fail in the same lots that had failures during the life tests. This would indicate that that reliability indicator test might be useful in indicating that a lot is a good candidate for flight qualification.

Voltage conditioning (for COTS lots without prior voltage conditioning heritage) was not found to be useful as a reliability indicator. The HALT results correlated fairly well; failing lots during HALT also had life-test failures. However, there were a couple of lots that tested well with HALT but also had life-test failures. The sample sizes and failure occurrences were not large enough to calculate an acceleration rate from the HALT data. More analysis of the HALT test for MLCCs was recommended.

The DPA results are still being evaluated, though the paper recommends continued use of DPA as a lot reliability indicator test because it seemed to correlate well with the life-test results, the method is highly standardized and repeatable, and it is fairly inexpensive to do. No correlation was found between the UVBS and the life-test results, and it was not considered a good reliability indicator test.

A second recent use of HALT by NASA to evaluate MLCCs occurred at NASA GSFC during a follow-up evaluation of parts identified for flight use. The parts were high-voltage chip MLCCs (rated for 500 V) from a single production lot. HALT was run at three voltage levels (a 150-sample set was split into three 50-piece groups): 1 kV, 1.25 kV, and 1.5 kV, all at 140°C. Insulation resistance was monitored as a measure of survival or failure with time. The failures were plotted using the Weibull method in order to find if separate and distinct failure regimes appear and to discover a failure rate. An MTTF equation was taken from reference [9] to determine whether the experimental data correlated with theoretically predicted behavior for MLCCs using a given test temperature.

The experimental data indicated that a single failure mode occurred. DPAs were successful in finding the failure site because they were very dramatic given the over-voltage test condition. The acceleration rate indicted by the data, however, did not agree with the theoretical estimate, and additional study is recommended.

Points of contact for HALT of MLCCs at NASA GSFC are Michael J. Sampson, Michael.J.Sampson.1@gsfc.nasa.gov; Jay Brusse, jay.a.brusse.1@gsfc.nasa.gov; and David Liu, dliu@pop500.gsfc.nasa.gov.

Wire-Bond Testing

The reliability of wire bonds in high-reliability microcircuits has been and continues to be of very high interest to project parts and reliability engineers. As recently as this year, critical flight system failure has been attributed to wire-bond failure. Wire-bond problems continue to come into the failure analysis laboratory at NASA GSFC as well. The mechanisms for wire-bond failure are varied; however, the majority tends to be related to incomplete weld between the bond-wire material and the bond-pad material or defects in that bond. The defects, typically voids, can be caused by the Kirkendall effect, which is related to relative diffusion rates between the materials. Alternatively the voids can be due to the Horsting effect, which is related to contamination either pre-existing at the bond site prior to bonding or that has migrated there after bonding. Excessive voiding or voids that group together make the bond weaker, which can lead to failure (see http://nepp.nasa.gov/wirebond).

High temperature (150 ºC and higher) is known to accelerate the growth of intermetallic regions between the bond pad and the bond wire, as well as any defects that are also developing. The standard burn-in and life test temperature of 125 ºC will often not effectively accelerate the intermetallic growth and lead to wire-bond failures within the limited time of the burn-in or life test. Therefore, the burn-in and life test may not always be effective in removing units that will have latent wire-bond failures.

Wire-bond strength has become a standard measure of bond quality. Bond strength can be measured non-destructively prior to device lidding or can be done destructively before or after lidding (on a sample basis). Standard accept/reject criteria and procedures have been developed for both approaches; however, both have disadvantages. They are considered to be labor intensive and require special attention to proper statistical sampling in order to determine lot wire-bond reliability. In-line, wire-bond quality assurance has become the norm in device manufacturing and assures wire-bond quality reducing the widespread use of bond-pull testing on finished lots. Problems can arise when procuring from a device manufacturer that does not have the production throughput to justify in-house process monitoring and also does not generate bond-strength statistics using lot-based bond-pull testing. It is even more difficult for the user if the vendor's quality system and production volume cannot be assessed adequately. This is a condition very common when procuring application-specific integrated circuits (ASICs) or parts from vendors who subcontract their packaging processes.

In the case of COTS parts, the user is not able, by definition, to require wire-bond testing and generally cannot view production-line quality processes or quality data. In the case of plastic encapsulated microcircuits (PEMs), the ability to pull bonds after receipt can be done only after the plastic has been chemically removed, which can significantly change the chemical landscape around the wire bond.

NASA GSFC has long been a regular user of ASICs that are packaged in-house at nearby research facilities such the Johns Hopkins Applied Physics Laboratory and through small-volume subcontracted manufacturing lines. The quality of the wire bonds in these parts is of great concern to the users; however, the opportunity to obtain the samples for proper destructive testing is very low. A new method for obtaining information that can correlate to wire-bond quality and ultimately to time to failure or life expectancy is being investigated to enhance NASA's ability to assess wire-bond quality for ASICs, PEMs, and similar parts.

To evaluate the reliability of wire bonds in ASICs (investigated for the GLAST project), the devices were subjected to high-temperature storage (HTS) at several temperatures. The degradation of the wire bonds was monitored using a forward voltage drop technique, which allows measurement of the changes in contact resistance during high-temperature storage.

The variation of contact resistance in wire bonds, Rc, was calculated based on forward voltage drop measurements of PN junctions used in the electrostatic discharge (ESD) protection circuits at the inputs and outputs of the device, before [$V_F(0)$] and after [$V_F(t)$] the temperature stress was imposed, using a constant forward current (I_F):

$$\delta Rc(t) = [V_F(t) - V_F(0)]/I_F$$

This technique does not require special test structures and allows for characterization of the wire-bond quality directly, without complex automatic test equipment (ATE) programming and without delidding or special part pre-processing.

At $I_F = 3$ mA, the values of $V_F(0)$ for the samples tested were in the range from 0.7 to 0.9 V. These values can be measured with an accuracy of 0.1 mV or better. In this case the accuracy of the Rc measurements would be ~0.03 Ohm. Temperature measurements for V_F have shown that the K-factor for these devices (the slope of V_F variations with temperature) was in the range from 2.3 to 1.5 mV/^{o}C, which is close to the value of 2.2 mV/ ^{o}C typical for silicon PN junctions. Considering possible temperature variations during measurements of $\pm$ 0.5 ^{o}C, the temperature-related error of Rc measurements would increase to ~0.25 to 0.35 Ohm.

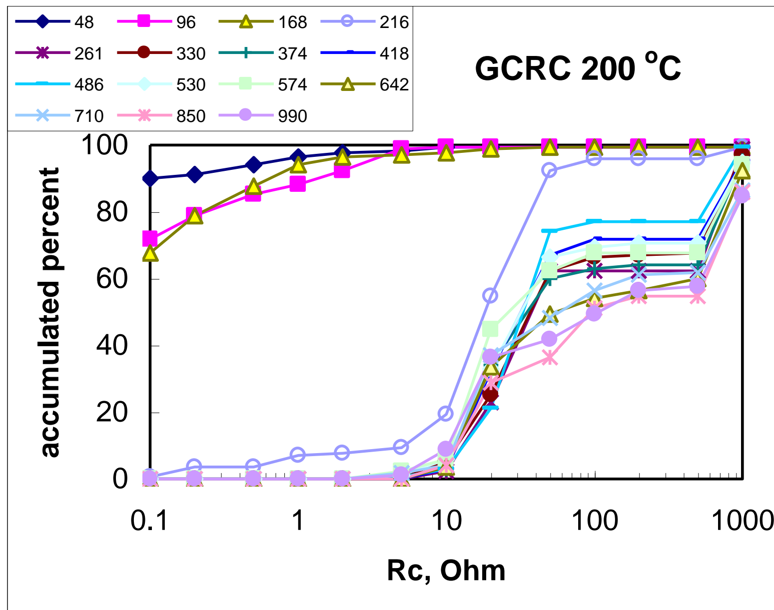
Initial values of Rc are in the milliohm range and the observed stress-related values were in the Ohms range. This allows the assumption, with a relatively high degree of accuracy, that the initial value of Rc can be neglected and that the contact resistance of a degraded bond is equal to its variation, $\delta Rc(t) \approx Rc(t)$.

Different groups of ASICs, in one of two types of packages, were stored at temperatures of 175, 190, 200, 210, and 225 ^{o}C for up to 2500 hours. The package styles were plastic quad flat pack (PQFP) with 80 pins (device called GCRC) and PQFP with 44 pins (device called GCFE). Three to five pieces were use in each temperature test group. The V_F measurements were carried out at room temperature periodically over the duration of the test. The total number of wire bonds measured in each group during HTS varied from 105 to 175.

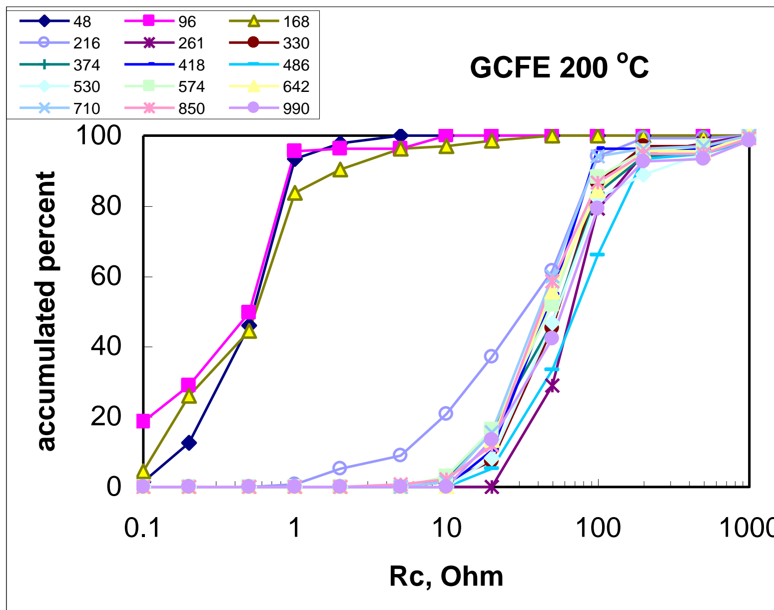
Rc was calculated for the V_F measurements that were taken periodically over the duration of the HTS. The data showed that there is a distinctive period of time in which Rc jumps from a low value around 1 Ohm to what is considered a failure, around and above 10 Ohms. Before this time, the distribution of Rc follows a curve with either a relatively small slope or a large slope, but in either case the curve lies to the left with the 50% accumulated percent value above and to the left of the (0.5 Ohm, 50%) coordinate. After the "jump," the curve shifts distinctly to the right, the slope increases, and the 50 accumulated percent (or higher) value is now above and to the right of the (9 Ohms, 50%) coordinate. The jump time can be observed only in this case based on the times chosen to take measurements. In this evaluation they were those times shown in Table 1, and the times were independent of the package type. Figures 1 and 2 show how the distribution curves had different shapes at different temperatures.

Table 1. Time Interval in Which the Rc Distribution "Jumps" From Mostly Passing to Mostly Failing the Rc Limit of 10 Ohms

HST Temperature	Test Duration Before Jump	Test Duration After Jump
175 °C	1679	1867
190 °C	328	444
200 °C	168	216
210 °C	72	96
225 °C	15	36

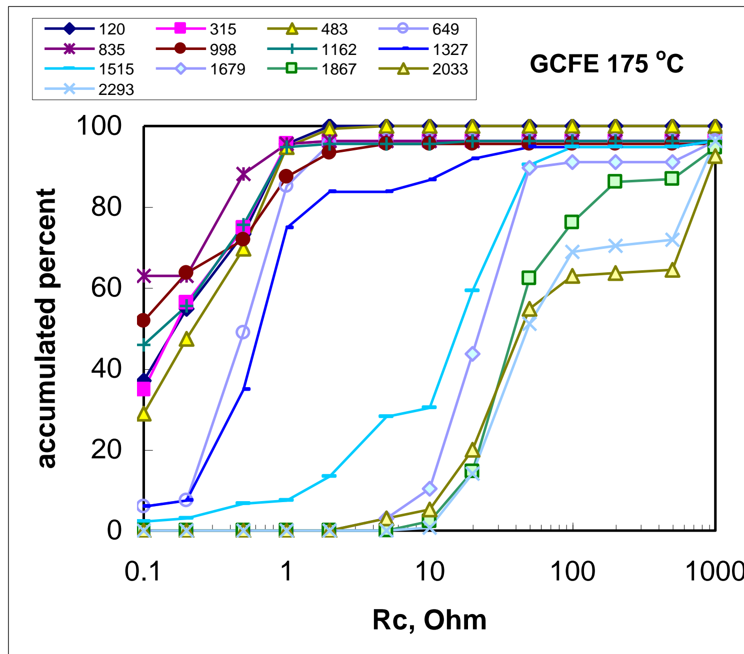


a. Example of pre-jump distribution having a relatively small slope. The post-jump distributions are somewhat bimodal.



b. Example of pre-jump distribution having a relatively large slope.

Figure 1. Examples of Rc Data



c. Pre- and post-jump curves are similar in slope and bimodal behavior emerges after 1515 hours.

Figure 2. Example of Rc Data

Using the assumption that an Rc ≥ 10 Ohms was indicative of a failure, the failure distribution was plotted using the Weibull method. From these plots, shape parameter (slope, β) and characteristic life (η) were determined and from those, activation energy was calculated (Figure 4). The characteristic life and shape parameter results were plotted in an attempt to find a linear dependence that could be used to extrapolate out a β and η for lower temperatures including 85 °C. With the extrapolated values it was concluded that the time to 0.01% failure for a group of 100 pieces, each with 100 wire bonds, was on the order of 1,000 years. The actual operating temperature of the spacecraft of 55 °C provided further assurance of wire-bond reliability.

Further work was done with this data set to examine the ability to predict infant mortality rates at reduced temperatures. Infant mortals were defined as all failures that occurred before the time of 0.01% failure for the population. The number of first failures (number failing the first time a measurement showed any wire bonds with Rc >10 Ohms) and the time of first failure were compared to the calculated time for 0.01% failure. There was only one failure that fit the definition of an infant mortal, and it occurred for the 80-pin group tested at 200 °C. This matched the experimental results and resulted in a failure density of ~0.2% for the 542-wire bonds in the sample group.

The assumption was made that the same activation energy could be used for both the lot reliability calculation and the infant mortality calculation, even though the related failure mechanism for normal life (wear out) and for premature failure (defect) was different. The 1.52 eV activation energy value was used to extrapolate the 48-hour failure in 200 °C to a time of failure for the same infant mortality in an environment of 85 °C. The result

was failure at 1,000 years. However, if a different activation energy were determined for the infant mortality case, such as 0.7 eV, that time of failure is reduced to 1.5 years.

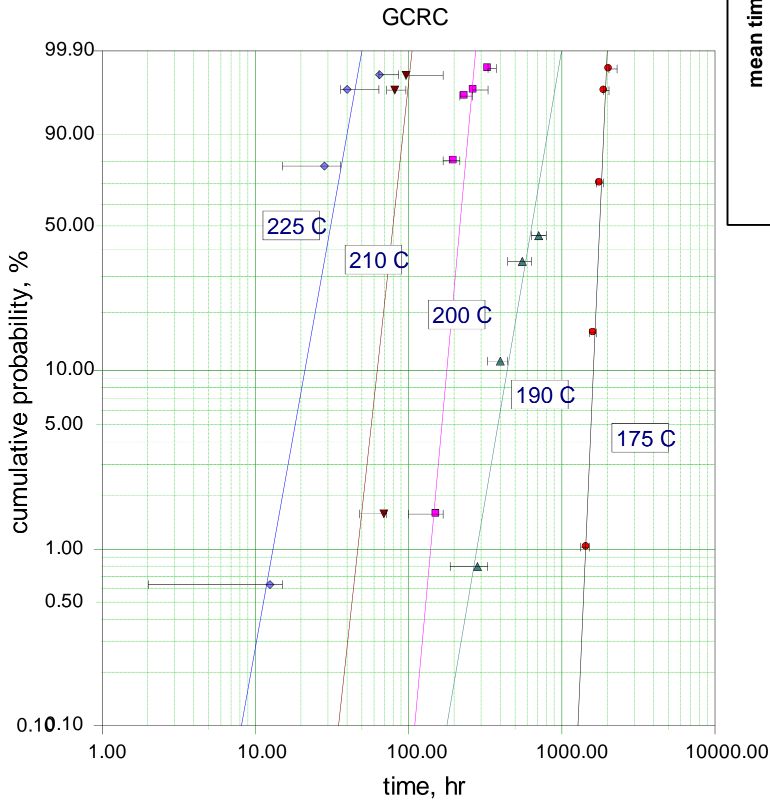


Figure 3. Example of Weibull Plot for Rc >10 Ohms

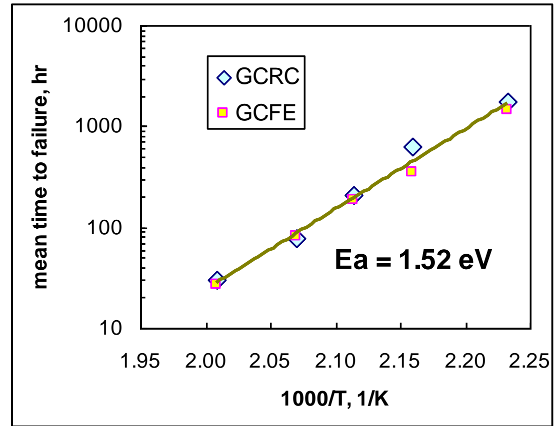


Figure 4. Activation Energy

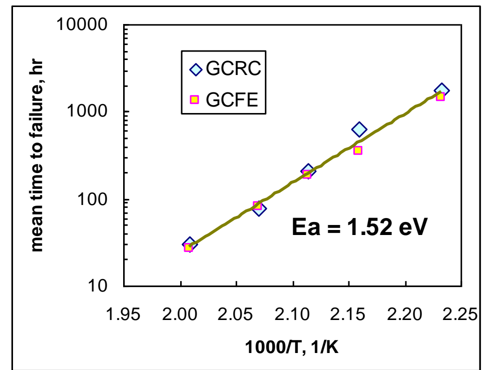


Figure 5. Shape Parameter Relationship to Temperature

Failure analysis of the early failures showed well-understood failure modes including uneven intermetallic (welding) coverage and voids in the intermetallic. There was no indication that there had been thermo-oxidation activity on or around the bond site, which was noted as supportive of the high activation energy value.

The voltage drop method for evaluating wire bonds was considered effective and will continued to be studied at NASA GSFC, especially with respect to what can be learned and predicted about infant mortal failures. More information on this topic can be learned from Alexander Teverovsky, ateverov@pop300.gsfc.nasa.gov; or Ashok Sharma, asharma@pop300.gsfc.nasa.gov.

HAST and Bias

Testing of a large number of samples (>31,000) of PEMs of several styles for a flight project in 2003 has provided NASA GSFC with some insight into some alternative test conditions to consider for PEMs. Following HAST (130°C/85%RH/250hrs), a 1.1% to 100% failure rate was found among the 44 lots that had previously shown a percent defective following burn-in of ≤ 5%. The MOSFETs were particularly vulnerable, as were thin-film resistors on op-amp chips. A more detailed investigation of the op-amp failures was performed through the use of the test flow shown in Figure 6.

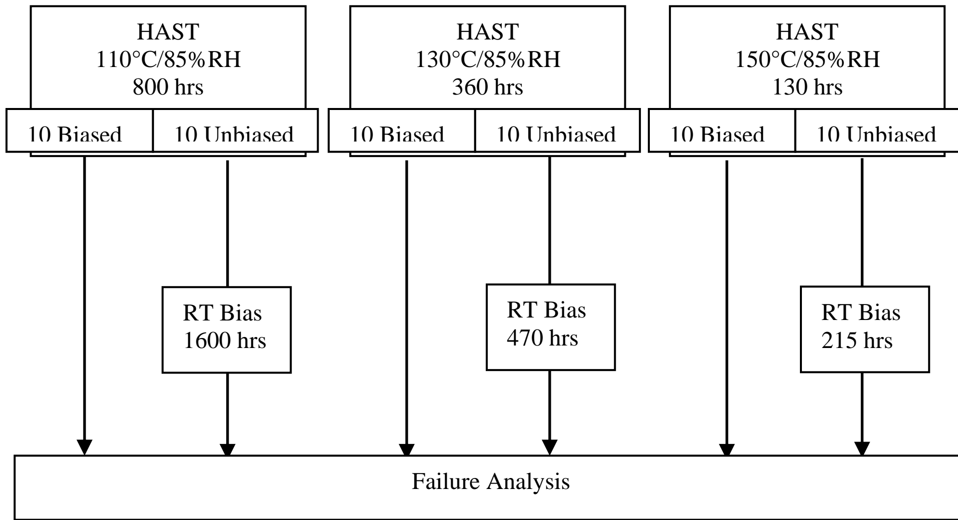


Figure 6. HAST Evaluation Flow

The results showed substantially more failures for the parts HAST tested with bias than without bias, but also showed failures for those HAST tested without bias and later biased for long periods on the bench. The failure distribution was plotted for the three temperatures for the HAST/bias samples (Figure 7), and an activation energy was calculated from the median time to failure for each temperature (Figure 8).

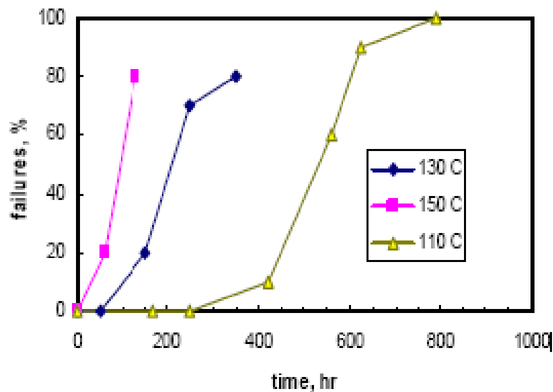


Figure 7. Failure Distribution Following HAST With Bias

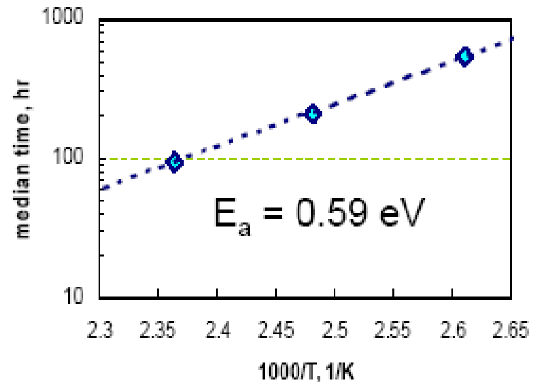


Figure 8. Activation Energy for HAST/Bias Failures

The resulting activation energy was fairly low (0.59 eV), indicating that the population tested would have a perceptible failure rate at lower temperatures, i.e., 1% after 2.2 years at 27 °C. The failure distribution after room temperature bias testing was not as straightforward to interpret; however, it might indicate that the failure mode is not distinctly temperature dependent (Figure 9), warranting further investigation.

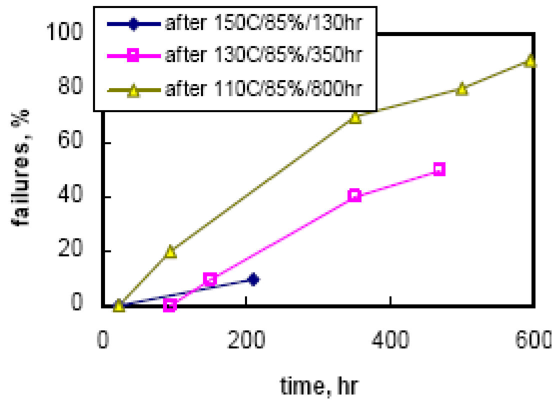


Figure 9. Failure Distribution Following RT Soak with Bias

Figure 10. Missing Thin-Film Resistor Material

Failure analysis showed that most of the failures had a section of chromium thin-film resistor missing (Figure 10). Dark field and scanning electron microscope examination revealed a crack below the missing material (Figures 11 and 12) in some of the samples. Further, it was noted that several defect sites (missing resistor material) were near aluminum metallization traces. These types of defects were found for both the samples tested with HAST/bias and with RT/bias.

Figure 11. Dark Field Image

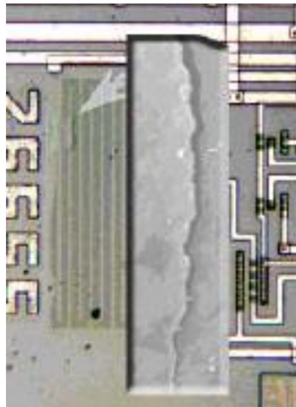


Figure 12. SEM Image Shown Next to Defect Location

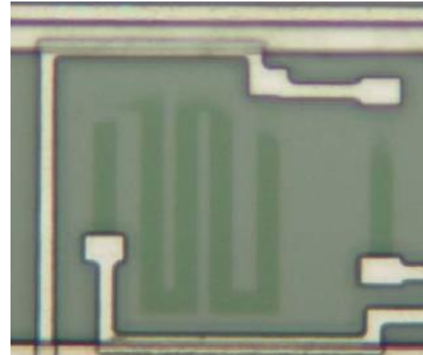


Figure 13. Defect Sites Near Aluminum Metallization

Consideration of the factors that would limit homogeneous disruption and damage to all of the Cr/Si resulted in identifying three: Diffusivity of the molding compound for moisture, galvanic corrosivity of the chromium, and diffusivity of the protective barriers

within the inner layers of the chip above the resistors (Si_3N_4 and SiO_2). Using representative and actual values for molding compound, Si_3N_4 and SiO_2 diffusivity, it is believed that the molding compound and the SiO_2 are relatively transparent to moisture (under 1,000 hours for complete saturation) at room temperature and above. In the presence of moisture, the leakage currents measured during testing and considering the dimensions and material of the resistor element, the thin-film resistors are expected to corrode. It is the moisture resistance of the Si_3N_4 that ultimately limits this failure mode. The mode under which the Si_3N_4 becomes defective is not fully determined, but it is hypothesized that stress from the proximity to the aluminum traces may be a factor.

The testing indicated that HAST and bias are useful for finding lots with defective internal passivation layers; however, these test may not be as dependent on temperature as originally thought. It also indicates that there may be some flexibility in how the tests are applied with regard to allowing the temperature and humidity conditions to be independent of the bias condition. More investigation of this theory is desired and will be performed by NASA GSFC as resources are available to do so. Further information about this work can be obtained from Alexander Teverovsky, ateverov@pop300.gsfc.nasa.gov; or Ashok Sharma, asharma@pop300.gsfc.nasa.gov.

Board-Level Testing

For many years, the aerospace community has been seeking ways to test assemblies and achieve electronic part assurance without piece-part evaluations. Several approaches have been explored through the NASA Electronic Parts and Packaging (NEPP) Program and are described in this section.

COTS Board Qualification

Board-level testing is especially advantageous to higher risk missions that are buying COTS boards where the opportunity does not exist to select and pre-process parts prior to board assembly. An examination of this approach was done through the NEPP program in 1998. Papers and presentations that came from this work are as follows:

1. "Assurance of COTS Boards for Space Flight – Part I," J. Plante, N. Helmold, C. Eveland, Commercialization of Military and Space Systems Conference, 1998.
2. "Working Draft – COTS Boards, Insertion Methodology and Plan, NASA GSFC – Code 562," Jeannette Plante, Swales Aerospace, 1998, http://misspiggy.gsfc.nasa.gov/tva/cots/insertplan.htm.
3. "Assurance of COTS Boards for Space Flight," J. Plante, COTS Journal, May/June Issue, 1999.
4. "Study of the Measurement Variation in IR Images of COTS Computer Boards," J. Plante, Swales Aerospace, September 1999, http://nepp.nasa.gov/DocUploads/47D23829-0C04-49AC-BB93BD7E74863FCF/cots_board_ir.pdf.

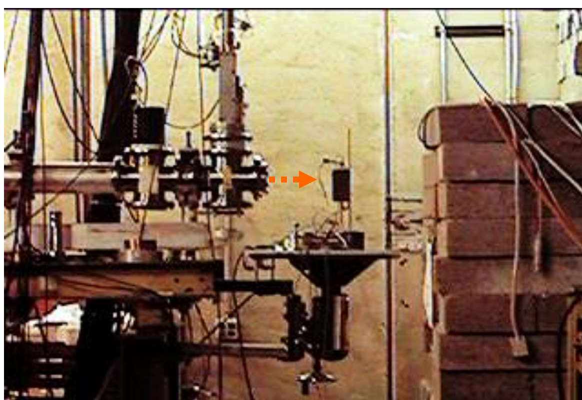
The emphasis was on procurement, board characterization including for radiation performance, considerations for mechanical testing, acceptance testing considerations, and ruggedization. A portion of the material is also dedicated to raising awareness about new assumptions users must make when they decide to work with COTS material.

Board-Level Radiation Testing
Contribution by Coy Kouba

NASA Johnson Space Center (JSC) utilizes the Indiana University Cyclotron Facility's (IUCF) 200 mega-electron-volt proton beam for the majority of its ionizing radiation testing. At this energy, it takes about 2.5 inches of solid copper to stop the proton beam. The test results are used to calculate an expected mean-time-between-failure (MTBF) rate for the device using a unique analysis tool called *PROTEST* (short for Proton-Test) developed by Dr. Pat O'Neill/JSC. This software takes the test data and integrates it with the International Space Station (ISS) space radiation environment. The output is the calculated MTBF rate expected for on-orbit operations.

Computer Circuit Card Being Tested at IUCF With High-Energy Particles
Figure 14.

Over the last year, JSC made 12 trips to IUCF, consuming over 250 hours of beam time. A wide range of electronic devices was tested, from MOSFET transistors to dynamic memories to field-programmable gate arrays (FPGAs). Most of the hardware was COTS technology, either as piece-parts or as complete commercial assemblies (such as a laptop computer). Much of the hardware tested was used to support various Shuttle Return-to-Flight projects, including digital cameras for the External Tank Thermal Protection System, components for the Orbiter Boom Sensor System, and the IBM A31P laptop computer and docking station. Other projects supported last year include wireless crew communication, personal digital assistants, miniAERCam, battery chargers, and ISS BioTech Facility components.



Sample Being Tested at IUCF With Low-Energy Heavy Ions
Figure 15.

When preparing for an evaluation, the JSC radiation test team meets with each project prior to testing to help them adequately prepare their hardware. The goal is to fully exercise the hardware in the beam, while monitoring the appropriate output responses to determine if errors or problems occur. The device must be functional and operated at a high duty rate, and in the same configuration as its intended spaceflight application. A

typical exposure for devices destined for use inside a pressurized ISS module is 600 rads (Si). This equates to about a 10-year proton exposure inside the module. The test data collected includes the number of errors that occurred, the nature of the error (i.e., system lockup, single bit-flip, output spike, etc.), and the recovery method required (automatic recovery, power cycle, etc.).

MTBFs for several devices tested this year include an Ethernet switch that upsets every 137 days of continuous use. An IBM docking station was tested and shown to have a permanent latchup failure in its power supply every 100 days. The IBM A31P laptop computer that was tested can be expected to upset every 36 days. For those devices that show no failures in a typical 600 rad (Si) exposure, it is estimated that the radiation MTBF will be greater than 10 years.

For more information contact Coy Kouba, 281.483.8069, coy.kouba-1@nasa.gov.

Board-Level Testing of PEMs

NASA GSFC has also examined board-level testing of PEMs. A typical part-level PEMs test plan includes electrical test, burn-in, temperature cycling, radiation tolerance, high-temperature operating life (HTOL), and HAST with humidity. Lead time and costs come with programming test equipment, building burn-in boards, performing electrical tests, and analyzing data. Board-level testing is suggested in the paper "Qualification of PEMs Using Board-Level Testing" by Alexander Teverovsky (http://nepp.nasa.gov/DocUploads/53F24459-4576-452E-B28E30C04F640651/Qualification%20system%20for%20PEMs%20using%20board1.doc). This board-level approach maintains this test flow structure though relegating some of the part-level tests to be done at the board level. In both of two options presented, it is assumed that individual parts are available to the evaluator and that inspections can be made at the part level such as DPA, visual, X-ray, and CSAM testing. The other tests are done at the board level either on test boards that are electrically representative of the flight board circuit (with sockets so that the parts can be removed and installed on flight boards) or on evaluation boards, also electrically representative, but not intended for use in flight hardware (disposable). These other tests include temperature cycling, surface-mount soldering simulation, HAST with moisture, power cycling, HTOL, electrical (functional) tests at high temperature, and radiation hardness.

Board-level test can be applied to boards that use a boundary scan design or a special representative evaluation board is provided. Testing is done with the involvement of the circuit designer in order to find critical failure modes. The boards are not yet conformal coated to enable part replacement if necessary, and spare boards are available for destructive testing.

Consideration must be given to the maximum operating temperature of the part or material on the board assembly with the lowest temperature rating. The paper recommends a 10 °C reduction in burn-in temperature from the maximum safe operating temperature of the entire board. To increase the test temperature in order to realize

failure acceleration, localized heating using foil heaters directly applied to the parts of interest is suggested. It is noted that behavior in temperature transition periods is a more informative observation than recording electrical measurements during dwell periods.

It is noted that there are no universally accepted methods for qualifying commercial parts for space use, so test plans should always carefully consider and reflect application conditions and mission priorities. Though test data is provided in this paper, the author considers it only in the context of the need for a continued study of this board-level approach.

Board-Level Testing of an FPGA at Low Temperature
(**Note:** This content was provided by Rajeshuni Ramesham of JPL and edited by J. Plante.)

The purpose for testing a Virtex-II board with the FPGA device installed at low temperatures was to discover whether the board and the device would survive and continue operating at different temperatures. Secondarily, an experiment was done to see whether the system could achieve a cold start or power cycle at –120 ºC. In doing this last maneuver, the FPGA was suspected to drain current on the order of 10 A.

The Virtex-II board was powered with three different independent power supplies. Voltages provided to the board were 3.3 V, 2.5 V, and 1.5 V. The 3.3 V (V_{ccaux}) was provided for the electronics in the board. The 2.5 (V_{cco}) provided power to the inputs/outputs (I/Os), banks, and rocket I/O transceivers. The 1.5 V (V_{core}) supplied voltage to the core.

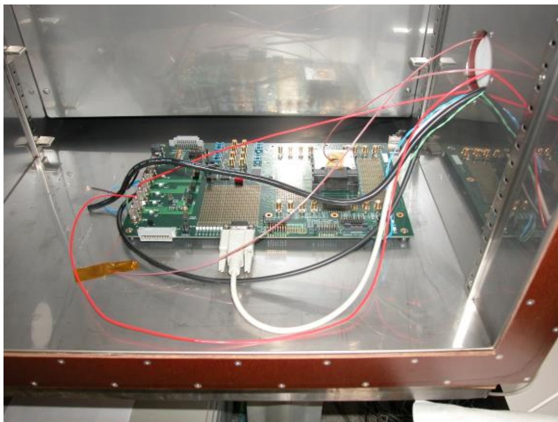


Figure 16a. Virtex-II Test Board in Temperature Chamber

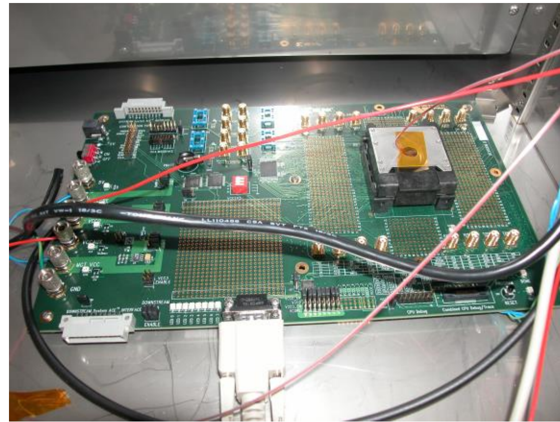


Figure 16b. Virtex-II Test Board in Temperature Chamber (Close View)

This part did not exceed the expectations of in-rush current. It was predicted to take up to 10 A but it ended up taking only about 220 mA. It is highly recommended that these tests be run again with considerably more time in the chamber to find out if this would make a difference in the in-rush current.

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The basis of accelerated life testing described in the Prokopowicz and Vaskas work is the equation below which establishes a relationship between MTTF t, testing voltage V, and temperature T.

$$(t_1/t_2) = (V_2/V_1)^N \exp[E_s/k(1/T_1-1/T_2)]$$

Where E_s is a pseudo-activation energy, N is the voltage acceleration factor, and k is the Boltzmann constant. Subscripts 1 and 2 refer to the test conditions 1 and 2, respectively.