Early Environmental Screening of Spacecraft Electronic Units using Pre-Unit-Level Thermal Testing

John W. Welch[1]
The Aerospace Corporation, 2350 El Segundo Blvd, El Segundo, CA 90245

Thermal test requirements for United States military spacecraft electronic units are specified in MIL-STD-1540. One of the primary objectives of this testing is to provide an effective stress screening environment for the detection of latent defects in flight hardware. Ideally, stress screening should be accomplished at the earliest test opportunity because late detection of design and workmanship defects can have a significant impact on hardware delivery schedules and program costs. Environmental testing standards, such as MIL-STD-1540, address screening at the unit level with the specification of test conditions typically more severe than what is expected in flight. When stress screening of electronic units is performed at a pre-unit level of assembly (e.g., printed wire board or slice), the test hardware can be screened more efficiently by detecting defects early, thereby increasing overall test effectiveness. In the latest revision of MIL-STD-1540, pre-unit-level thermal testing of electronic units is an option to the baseline test approach and may result in the relaxation of unit-level thermal test requirements. This paper discusses the implications of pre-unit-level thermal testing of electronic units and how these tests can be designed to effectively meet test objectives.

Nomenclature

ESS	=	Environmental Stress Screening
F_T	=	total number of failures found in a test(s)
F_A	=	total number of failures available to be found including early flight operations
MPT	=	minimum to maximum predicted temperature range
N	=	number of cycles performed
N_{Equiv}	=	number of equivalent cycles
T	=	test temperature range
T_{1540}	=	required unit temperature range
TE	=	test effectiveness

I. Introduction

For United States military space and launch vehicles, MIL-STD-1540E, released as SMC-S-016 [1] and TR-RS-2014-00016 [2], requires thermal testing of electronic units with the primary objectives of accruing environmental stress screening (ESS) to precipitate latent defects into observable failures and demonstrating mission functionality, operation, performance, survival and turn-on requirements. The thermal test requirements that accomplish the ESS objective subject the spacecraft unit to physical stresses more severe than that expected in flight to ensure detection of a majority of the unit's infant mortality failures sensitive to particular test environments. This is justified in that a space vehicle's storage and mission life are nearly always greater in duration than the time spent in ground testing and ESS. The physical stresses associated with wide temperature ranges and multiple cycles and the duration spent in these thermal test environments make a high test effectiveness possible.

The thermal tests that comprise a unit thermal program are the thermal cycle test, thermal vacuum test and burn-in test. Thermal cycling subjects the unit to multiple temperature cycles in an ambient pressure environment with the primary objective of ESS. Thermal cycle testing has been found to be the most perceptive of all ground tests for screening effectiveness [3]. Thermal vacuum testing subjects the unit to vacuum with the same test temperature

[1] Associate Director, Spacecraft Thermal Department, M4-916.

range as the thermal cycle test but fewer cycles with a primary objective of demonstrating performance in a flight-like environment. Although not to the same test effectiveness as the thermal cycle test, the thermal vacuum test accomplishes ESS with an emphasis on vacuum-sensitive failure mechanisms. Burn-in testing is a continuation of the thermal cycle test environment with the unit subjected to either temperature cycles or a constant hot test environment. The test ensures that units are subjected to a consistent number of hours of thermal testing with the primary goal of ESS.

Test effectiveness has been defined as a quantitative measure to evaluate and compare ground testing environments [4]. It considers failures found during a particular test environment, failures found in a comprehensive test program, and failures found during early flight operations. The definition of test effectiveness for a particular test is the quotient of two parameters: the number of failures found in that test divided by the total number of failures available to be found. This latter term includes failures found in that test, in all subsequent ground tests and during early flight. Early flight operation is typically specified as the first 30 to 45 days after launch or after the unit has been turned on in flight. As provided in [4], the test effectiveness is,

$$TE = \frac{F_T}{F_A} x\ 100 \tag{1}$$

where,

TE = test effectiveness for the test(s) of interest
F_T = total failures found in the test(s) of interest
F_A = total failures available to be found including early flight operations

With this equation, the important parameter in determining the test effectiveness is the number of failures found in that test. As the number of failures detected increases, the test effectiveness of that test increases. From an ESS perspective, this is an acceptable approach provided test parameters are adequately stressing to precipitate defects into observable failures, test parameters are consistent across test programs, and tests are perceptive at detecting failures as they occur. General statements about an environmental test's effectiveness are only valid if the key test parameters in that test (number of cycles, test temperature range, test duration) are uniformly established at stressing levels and functional tests are perceptive enough to detect defects.

Another factor that may affect the test effectiveness is the order in which ground testing is conducted. Thermal tests, with their long test durations and number of functional tests performed, are inherently effective at detecting problems as they become apparent. Tests performed at the end of an environmental test program may have a lower test effectiveness as compared to those conducted at the beginning of the test program.

When an environmental test is conducted and no failures are detected, this can imply one of several possible assessments:

1. The test parameters were not stressing enough to force latent defects into failures
2. The test perceptiveness was not thorough and thus test failures were not detected
3. The flight hardware was not sensitive to the test environment
4. The flight hardware was of high quality and there were no failures to be found in this test

The first two reasons are the fault of test planning and result in undetected failures that may be found in subsequent ground testing or in flight. The third reason is an assessment of the nature of the failure mechanisms associated with the ground test and how they relate to the flight unit while the fourth reason is a verification of flight-worthiness. In all four cases, a test effectiveness as computed by Eq. (1) is zero, but the reason for the effectiveness may not be obvious. A common response from test conductors and customers alike is that when a test finds no defects, it can be concluded that the hardware is of high quality and conducting the test was unnecessary. It may be entirely true that the hardware is of high quality, but finding no defects from a well-planned and well-executed test is still necessary to verify this statement. A more thorough assessment of the test execution and test results may reveal that either of the first two reasons above may have been likely. Furthermore, if the assessment can clearly show that the test hardware is not sensitive to the test environment (third reason), then test elimination may be considered.

A shortfall of Eq. (1) is that it has been used to assess a test's value solely based upon its ability to detect latent defects. While this test objective is clearly important, it is not the only consideration that should be made in comparing ground tests. Besides ESS, unit testing also meets test objectives related to verification of mission performance requirements and turn-on and survival capabilities. A ground test that detects few failures but provides insight into the performance and operation of test hardware can hardly be called ineffective. This is especially true for the thermal vacuum test which combines temperature and vacuum environments to test hardware in the most flight-like of all ground tests [5]. As compared to the thermal cycle test, its test parameters are not highly stressing (fewer cycles and smaller temperature transition rate), but thermal vacuum testing provides invaluable data for

assessing mission capabilities. This is evidenced by the duration of performance testing conducted in the thermal vacuum test, particularly at the space vehicle level.

With this understanding as a background, the focus of this paper is a tailoring option in MIL-STD-1540 to improve the ESS effectiveness of a unit-level test program for electronic boxes by conducting enhanced thermal testing at an earlier level of assembly. The current baseline requirements for unit-level testing of electrical and electronic units, as provided in MIL-STD-1540E, specify thermal cycle, thermal vacuum and burn-in testing to the duration and temperature ranges shown in Table 1 for qualification, protoqualification and acceptance hardware.

Table 1. Thermal Test Parameters Required in MIL-STD-1540E for Electrical or Electronic Boxes

Hardware Level	Test Cycles	Test Temperature Range
Acceptance	14 cycles	MPT, or -24 °C to +61 °C, whichever is more severe
Protoqualification	20 cycles	MPT ± 5 °C, or -24 °C to +61 °C, whichever is more severe
Qualification	27 cycles	MPT ± 10 °C, or -24 °C to +61 °C, whichever is more severe

MPT: Minimum to Maximum Predicted Temperature Range (model predictions ± thermal uncertainty margin)

The baseline thermal test program for an acceptance electronic unit would consist of 10 thermal cycles plus 4 thermal vacuum cycles. If this testing did not exceed 200 hours, burn-in testing would be added to achieve the 200 hours of total thermal test time. The test temperature range begins with a computation of the minimum to maximum predicted temperature range (MPT, model temperature prediction range ± 11 °C thermal uncertainty margin) and compares this range to a default screening temperature range of -24 °C to +61 °C. Acceptance testing is established by selecting the enveloping values of these ranges. For example, if a unit's MPT is -10 °C to +65 °C, the acceptance test range would be -24 °C to +65 °C. In thermal cycle and thermal vacuum testing, performance tests are conducted at hot and cold temperature plateaus (-24 °C and +65 °C in the previous example) on the first and last cycles and functional tests are conducted at these temperatures on intermediate cycles. Burn-in testing is conducted either cyclically over this temperature range or held constant at the hot acceptance temperature. The multiple cycles over this temperature range are regarded as the most important thermal test parameters for achieving desired ESS [6].

Thermal testing at subsequent levels of assembly (subsystem and space vehicle) is conducted with an emphasis on demonstrating mission performance requirements, verifying interfaces between subsystems, understanding operational end-to-end functionality and demonstrating mission readiness. There is less emphasis on ESS for several reasons. At higher levels of assembly, it is difficult to subject flight hardware to the necessary thermal stresses to achieve a rigorous ESS. The mass of a space vehicle prevents high temperature transitions rates and subsystem interaction and vehicle complexity make perceptiveness difficult. Inclusion of thermal control features (heat pipes, heaters, etc.) makes achieving a wide temperature range nearly impossible. For these reasons, space test programs have emphasized ESS at the unit level of assembly and performance verification in a flight-like environment at higher levels of assembly. This has not completely eliminated finding unit defects in higher level testing, but it remains the goal.

Testing at the earliest possibility enables defects to be corrected with minimal interference from a hardware and from a program perspective. When caught early, failures are easier to isolate, repair and retest with less impact to program cost and schedule. The lowest level of assembly for which MIL-STD-1540E specifies requirements is the unit level. The Standard assumes that ESS is being performed at lower levels of assemblies (piece parts, boards, slices, etc.) and that high-quality hardware, properly tested, comprise a spacecraft unit. Contractors and vendors use their own internal requirements and command media and practices to specify the rigor of lower level testing. In the past, prime contractors were typically the manufacturer of a vehicle's electronic boxes so there was relative consistency between units in how parts and printed wire boards were tested. In recent years, there has been an increase in box manufacturing by subcontractors and less oversight by the prime contractor regarding processes and test execution. While there are no data to indicate a higher return rate for this trend, there is less consistency in how lower level testing is accomplished.

In the most recent release of MIL-STD-1540E [1-2], tailoring options have the intent of maintaining the same mission risk while offering possible savings in test program costs. One such option is to grant credit toward unit-level thermal testing requirements when thorough pre-unit-level (board, card, or slice) thermal testing is accomplished. Testing at the lower level would help meet ESS objectives in an efficient manner and the credit given at the unit level would be in terms of a test cycle requirement reduction. The customer would benefit from such an option in that minimum ESS test objectives are still being satisfied and greater visibility is gained into the testing conducted at lower levels of assembly. The purpose of this paper is to discuss the proposed test option for pre-unit-level thermal testing, rationale for such testing, and how the test option might be implemented.

II. Pre-Unit-Level Thermal Testing Option Description

For this option to be taken and a credit granted toward unit-level thermal testing, the following criteria need to be satisfied [2]:

a. Slices/boards shall be powered on and monitored during testing.
b. All slices, boards, and cards in a unit shall be tested in the same manner. Temperature levels (average values at the same relative locations) shall envelope (hot and cold) those at the unit level.
c. Performance and functional testing, as appropriate, shall be conducted during the first and last cycles of slice/board thermal tests at hot and cold temperature plateaus. Perceptive parameters shall be monitored during all other phases of the tests.
d. Slice/board thermal test plans and procedures shall be documented in a manner similar to unit-level thermal testing.
e. Slice/board thermal test results shall be documented and approved by the customer. The reports shall address all anomalies, failures, corrective actions, and observations found during the test.
f. An assessment shall be made on all items or aspects of the unit not subjected to slice/board thermal testing (interfaces, connecting cables, subassemblies not mounted to boards, parts mounted to chassis walls or base plate, etc.). This assessment shall consider the integrity and robustness in meeting unit level design and performance requirements as these items are exposed to fewer unit cycles when the slice/board thermal test credit is taken.

If the above criteria are satisfied and approved by the customer, unit-level test credit shall be applied to the thermal cycle test and burn-in test requirements (not thermal vacuum test) in that the required number of unit-level thermal cycles and the burn-in test duration shall be reduced. The maximum cycle credit given for slice/board level thermal testing shall be half the required number of unit thermal cycles. For example, an acceptance unit requiring 14 thermal test cycles (ten thermal cycles and four thermal vacuum cycles) may be given a seven-cycle maximum credit for slice/board level testing, and the unit thermal cycle test program is modified to three thermal test cycles and four thermal vacuum test cycles.

When slice/board temperature ranges differ from required unit level test ranges, a relationship provided in MIL-STD-1540E may be used to compute equivalent test cycles. The relationship is intended to provide a similar low-cycle fatigue exposure by increasing the number of test cycles when the test temperature range is less than the MIL-STD-1540 requirements. The expression can also be used to calculate the number of equivalent cycles for the purpose of comparing screening exposure. The relationship is,

$$N_{Equiv} = N\left(\frac{\Delta T}{\Delta T_{1540}}\right)^{1.4} \tag{2}$$

where,

N_{Equiv} = number of equivalent cycles
N = number of cycles performed
ΔT = test temperature range (in °C)
ΔT_{1540} = required unit test temperature range (acceptance range in MIL-STD-1540: ΔT = 85 °C)

The slice/board with the fewest number of equivalent unit-level cycles shall be used for determining the cycle credit to be taken. For example, a three-slice unit with three, seven, and ten equivalent unit-level cycles shall be given a three cycle credit in reducing unit cycle requirements. Likewise for the burn-in duration credit, the slice/board with the minimum equivalent thermal test hours shall be used for determining the unit-level burn-in credit. Duration hours count only when the slice/board is powered on in the slice/board test. Unlike the thermal cycle credit, the minimum equivalent duration of slice/board testing that meets the above criteria may be sufficient to eliminate the need for any unit-level burn-in testing when the number of accrued hours in slice/board testing meets or exceeds the number of hours required at the unit level and when all critical unit hardware has been subjected to adequate slice/board testing.

Slice/board level thermal testing shall not eliminate or reduce other unit thermal requirements (e.g., failure-free cycles, survival demonstration, dwell times, etc.) to be demonstrated in unit thermal tests.

III. Discussion of Pre-Unit-Level Thermal Testing Option

The pre-unit-level thermal testing option was developed following recognition that space vehicle contractors were acknowledging the benefit of early screening of electronic units but were inconsistently conducting thermal tests at this level of assembly. Some tests were conducted with units powered off, contractors were asking for unit screening credit when only a couple of the boards in a unit were tested, and some tests were performed with no reporting of test failures that occurred in the tests. It was felt that with consistent testing techniques similar to what would be done in unit-level thermal testing, credit could be given to reducing the test cycles in unit thermal tests because screening goals were being accomplished in the pre-unit-level testing. From a customer perspective, MIL-STD-1540 defines a minimum screening level for electronic units. If a portion of this screening is being accomplished in pre-unit-level testing, then it should reduce the required screening at the unit level. The criteria are proposed to ensure that the pre-unit-level screening is being accomplished properly.

When this option is invoked and the criteria are satisfied in pre-unit-level thermal testing, each board or slice is subjected to thermal cycle testing (or thermal vacuum testing if desired) with multiple cycles over a test temperature range that is at least as wide as the unit test temperature range. Following a complete pre-unit-level thermal test program, the unit is assembled and subjected to a unit thermal test program with a reduced number of test cycles. The test duration is reduced with no other changes to unit-level test parameters (e.g., the unit test temperature range remains unchanged). The option is applicable to acceptance of electrical and electronic units only because qualification and protoqualification (and protoflight) units have design verification objectives in addition to screening objectives and these design objectives may require additional unit cycles to demonstrate compliance. This option is not applicable to mechanical units because the primary purpose of thermal testing of these units is performance verification in a flight-like environment and not environmental stress screening [7] and as a result, far fewer cycles are required.

For pre-unit-level thermal testing, the only test parameter with a requirement is the test temperature range; it should be at least as wide as that conducted for unit-level thermal testing. There is no requirement for the number of test cycles, in that they may be more or less than the number of unit-level test cycles. In pre-unit-level testing, (1) thermal dwell may be shorter because of reduced thermal mass, (2) thermal soak may be shorter because less performance and functional testing is conducted, and (3) temperature transitions rates may be greater because of less thermal mass. Furthermore, hot and cold starts and demonstration of failure free cycles are not required in pre-unit-level thermal testing.

The cycle credit in pre-unit-level thermal testing may reduce the total number of cycles in the thermal cycle test by as much of half and potentially eliminate unit burn-in testing. There is no credit given to the unit thermal vacuum test because the number of required cycles is only 4 and if the unit thermal vacuum test is necessary to demonstrate vacuum-related issues with the unit, then 4 cycles is required. An example is given in MIL-STD-1540E where an electronic unit has an acceptance test program that consists of both thermal cycle and thermal vacuum testing. This and other examples are given below.

(1) Unit thermal testing consisting of thermal cycling and thermal vacuum testing. When an acceptance unit test program consisting of 14 thermal cycles (10 cycles in thermal cycling and 4 cycles in thermal vacuum) conducts pre-unit-level thermal cycling that meets the criteria given, the number of thermal cycles (14) is reduced in half (7) resulting in a test program consisting of 7 cycles (3 cycles in thermal cycling and 4 cycles in thermal vacuum testing).

(2) Unit thermal testing consisting of thermal cycling only. For an acceptance unit with a test program consisting of 14 cycles (14 cycles in thermal cycling), reducing the number of thermal cycles in half results in a test program consisting of 7 cycles (7 cycles in thermal cycle testing).

(3) Unit thermal testing consisting of thermal vacuum only. For an acceptance unit with a test program consisting of 14 cycles (14 cycles in thermal vacuum testing), reducing the number of thermal cycles in half results in a test program consisting of 7 cycles (7 cycles in thermal vacuum testing). This reduction is not in conflict with an earlier statement in this paper about no credit given to thermal vacuum testing because the reduced test program still consists of at least 4 cycles.

(4) Burn-in credit. For an acceptance unit with a 200-hour burn-in requirement in unit testing, if the minimum number of hours accrued in any single pre-unit-level thermal test is 40 hours and the unit-level testing (thermal vacuum and thermal cycling) accrues 160 hours, no additional unit-level burn-in testing is needed.

The credit is computed by normalizing all pre-unit-level thermal testing to equivalent testing at unit-level thermal test requirements (cycles and temperature range) using the relationship provided by Eq. (2). Consider a unit consisting of three slices: (1) Slice A had slice testing conducted over a 105 °C temperature range for 10 cycles, (2)

Slice B had slice thermal testing over a 95 °C range for 15 cycles, and (3) Slice C had slice testing over an 85 °C range for 20 cycles. Using Eq. (2), equivalent cycles to the MIL-STD-1540E range would be: Slice A = 13.4 cycles, Slice B = 17.5 cycles, and Slice C = 20 cycles. From a perspective of equivalent fatigue exposure, a 10-cycle test over a temperature range of 105 °C has the same screening effectiveness as a 13.4-cycles test over an 85 °C temperature range.

In computing the reduction credit, the slice with the minimum number of equivalent cycles is used. In the previous example, Slice A had the smallest N_{Equiv}, but because this value is greater than 7, the number of cycles in unit-level thermal cycling may be reduced from 14 to 7. If N_{Eqiv} had been less than 7, then the number of cycles in unit-level thermal cycling would have been reduced by N_{Equiv}. For burn-in testing, a similar method is used but without the use of Eq. (2) and with operating time. The slice with the smallest duration of operating time is used to compute the burn-in credit. Only operating time in pre-unit-level testing is considered and would not include time with the unit off (for temperature transitions or for anomaly resolution). As previously stated, the minimum pre-unit-level operating time can be used to completely eliminate unit-level burn-in testing if this value when added to the duration of unit-level thermal testing (thermal cycling and thermal vacuum) exceeds the burn-in duration requirement. A note of caution is appropriate here: if a number of devices in the unit are not being screened in pre-unit-level thermal testing, then it may be prudent to maintain the unit burn-in duration requirement (200 hours in MIL-STD-1540E) to ensure that all unit hardware has been properly screened in burn-in testing.

Pre-unit-level thermal testing only changes the number of unit-level thermal cycles. It does not change the value of other test parameters (e.g., test temperature range, the thermal dwell time, thermal soak times, and the temperature transition rate) in the unit thermal test. These parameters are maintained at the unit-level specification requirements. The maximum reduction in the number of cycles performed in unit-level thermal cycling is 7 cycles, so for acceptance testing, the unit thermal cycle test profile reduces from a 10-cycle test to a 3-cycle test. Performance tests are still conducted at hot and cold temperatures on the first and last cycle, so the unit-level test reduction is to intermediate test cycles only. A depiction of a baseline MIL-STD-1540E unit test profile for a unit with thermal cycling only along with the pre-unit-level thermal testing option invoked is shown in Fig. 1. Notice that only the intermediate cycles are eliminated when pre-unit-level thermal testing is performed.

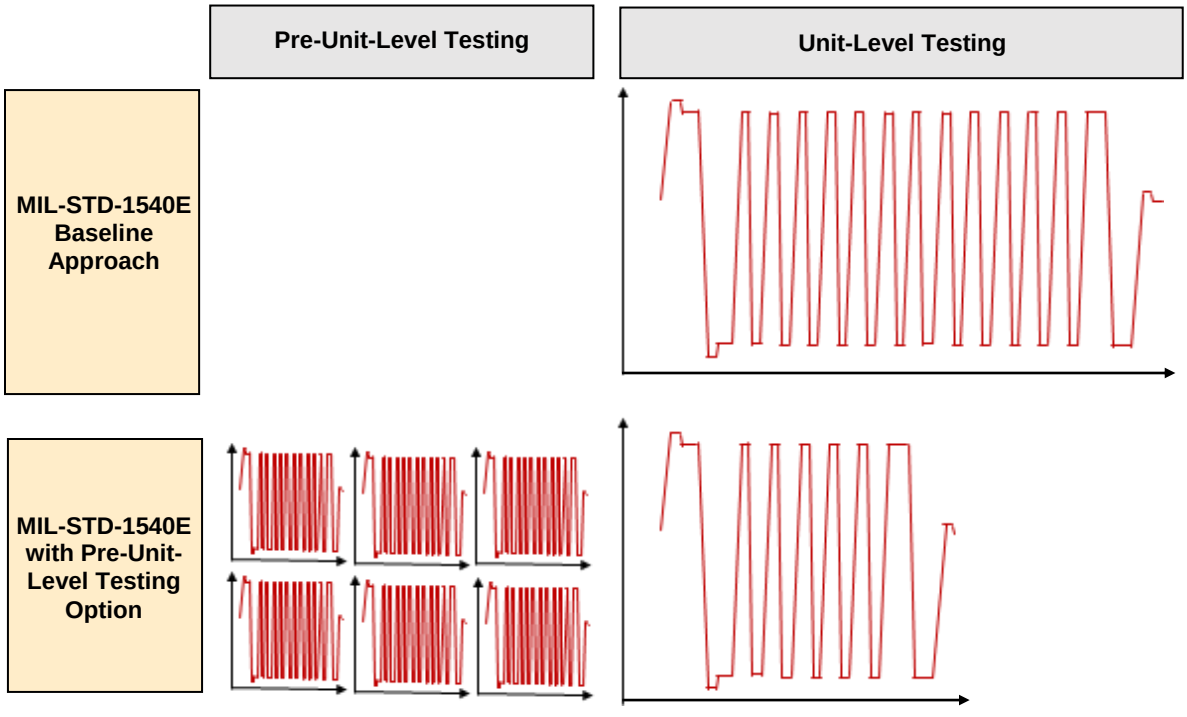

Fig. 1. Comparison of Baseline MIL-STD-1540E Unit Test Profile (Thermal Cycling Only) with Pre-Unit-Level Testing Option Test Profile

IV. Rationale for Pre-Unit-Level Thermal Testing Option

Section II of this paper begins with the criteria that must be satisfied to earn the unit-level thermal test reductions. Compliance to the criteria helps ensure that pre-unit-level thermal testing is being conducted uniformly across the unit and in a manner similar to unit-level testing expectations.

Criterion (a) states that all slices or boards are to be powered on and monitored during testing. This is consistent with unit-level testing requirements, increases the ESS effectiveness, and enables functional testing of the slice or board. Activating the slice or board will simulate thermal gradients between piece parts and the mounting surface in a similar manner as expected in the unit thermal cycle test. It also increases temperatures of piece parts and thermal gradients across connectors and joints, improving screening effectiveness. Finally, turning the hardware on enables functional measurements to be made to compare with expected performance requirements.

Criterion (b) states that all slices, boards and cards are to be tested in a similar manner. There are two points of importance in this criterion. The first point is emphasis on the word "all". A pre-unit-level test program cannot test half of the slices in a unit and then claim the cycle credit at the unit level. The reason for this is that completion of a unit's pre-unit-level thermal testing assumes that an established screening effectiveness has been met for all the boards and slices in the unit and that the level of screening effectiveness can be essentially subtracted from the screening that needs to be accomplished at the unit level. The second point is that all pre-unit-level thermal testing is to be conducted in a manner similar to unit-level testing. The example is given that temperature levels for the board or slice testing need to envelope the unit-level test temperature levels. This implies an assumed condition that pre-unit-level thermal testing will use test parameters, namely test temperature ranges and temperature transition rates that may be more stressing than what will be experienced in the unit-level thermal test (without overstressing slices and boards). Test procedures, test profiles and methodologies should be similar to unit-level testing and consistent between all pre-unit-level thermal tests.

Criterion (c) addresses what is expected functionally from the slice or board-level test. While the unit is operating, perceptive parameters (output measurements) should be monitored during all phases of the test. This is consistent with the requirements for unit-level testing. At temperature plateaus, performance tests should be conducted to ensure that the unit is performing within expected mission requirements. This means that during test planning, responsible unit engineers need to determine the performance measurements that can be made for each board/slice and the perceptive parameters to be monitored throughout the test. The engineers will also need to develop test scripts to run at hot and cold temperature plateaus to make these measurements. In many respects, the pre-unit-level thermal test will resemble a unit thermal test, but with less complex test hardware and shorter duration test scripts. The words "as appropriate" are included in this criterion to acknowledge that there may be some boards or slices that do not have measurable outputs that can assess board performance or functionality. In such cases, the board/slice is to be cycled through its different operating modes throughout the test.

Criterion (d) stipulates that test planning and documentation should be similar to that expected for unit-level testing. Test procedures and test plans should be formally documented and provided to the customer prior to testing. Any "red-lines" made to the procedures prior to the test or during the test need to be approved by the customer. The procedures should have entrance and exit criteria as might be found in a unit test procedure and the course of action for test anomalies should be clearly stated in the test plan.

Criterion (e) addresses expectations for a test report following the test. Similar to the Criterion (d), post-test documentation should be similar to what would be submitted following a unit-level test. The report is formal documentation of the test and should be approved by the customer. It reports how the test met its exit criteria and documents any observations, failures and anomalies, how these events were dispositioned and what corrective actions were taken. Root causes (or paths toward root causes) for these observations should be discussed.

Criterion (f) is an acknowledgement that there may be hardware that will not be subjected to board/slice-level testing. These devices include parts not mounted to a board or slice (e.g., modules or power supplies), parts mounted directly to the unit baseplate or chassis wall, devices at board interfaces, and cables or harnesses that mount between boards or are not associated with a particular board or slice. For these devices, an assessment is required that addresses the robustness of these hardware in meeting their design and performance requirements with fewer test cycles in unit-level thermal testing. If these devices can demonstrate robustness through previous testing or ample design margin, then the program risk of these devices seeing no pre-unit-level thermal testing and reduced screening in unit thermal testing may be considered acceptable. If these devices cannot demonstrate this robustness, then these devices should be included in an existing slice/board level test(s) to accrue additional screening or the number of unit-level thermal cycles cannot be reduced

When the criteria are correctly applied, the number of thermal cycles in the unit thermal cycling may be reduced in half. Rationale for this half-credit is subjective in that it is not based upon test data. Rather it is reasoned that pre-unit-level thermal testing can never accomplish all of the objectives of unit-level thermal testing, in that it cannot demonstrate unit performance or functionality, slice-to-slice performance, slice interfaces, unit thermal performance (e.g., baseplate conduction), and performance of devices not mounted on slices or boards. These verifications are important enough to justify a meaningful unit-level thermal test program regardless of how much screening is accomplished in lower level testing. Therefore, justification for the half-credit is a balance between encouraging formal pre-unit-level thermal screening while satisfying unit-level thermal test objectives.

According to Welch and Wright [8, 9], an acceptance unit thermal test program consisting of 14 thermal cycles over a temperature range of 85 °C has historically demonstrated a test effectiveness of about 95%. This is shown in Fig. 2 where the curve indicates a test effectiveness of about 96% at 14 cycles. The curve shows that below about 10 cycles, test effectiveness decreases sharply with a reduction in test cycles. Based upon these data, if thermal cycles are reduced to 7 cycles, the test effectiveness would decrease to about 83%. The difference between this value and 100% represents the likelihood of latent defects escaping into higher levels of testing. As a result, testing to 7 thermal cycles is a four-fold (17 percent as compared to about 4 percent) likelihood increase in the number of unit-level defect escapes into vehicle-level testing or flight. There is also increased uncertainty with the 83% value due to the slope of the curve at 7 cycles. Nevertheless, it was assumed in development of this test option that pre-unit-level thermal testing can compensate for this test effectiveness reduction since the combined slice/board testing with unit testing can result in a test effectiveness equal to or greater than that shown for 14 cycles.

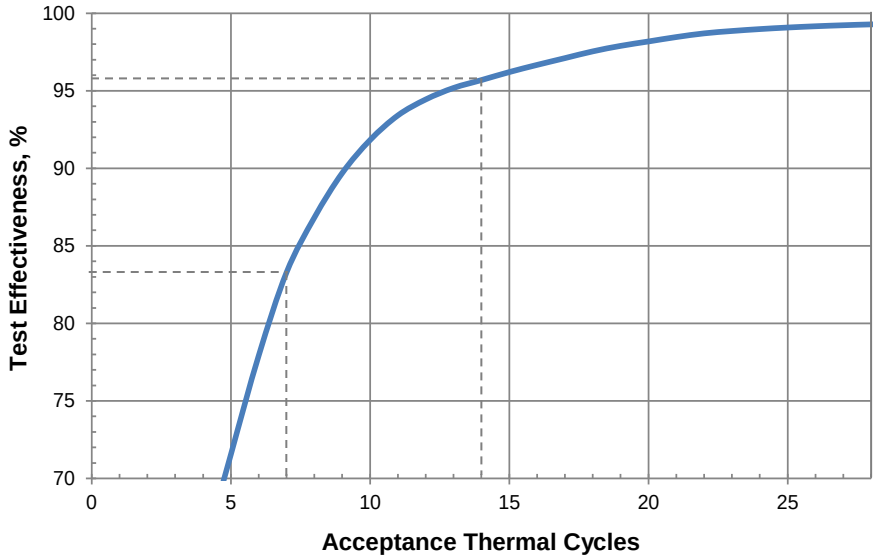

Fig. 2. Test Effectiveness as a Function of Acceptance Unit Thermal Test Cycles (Temperature Range of 85 °C)

For devices that are not tested in slice/board thermal testing (e.g., attached to the baseplate), the assessment required in Criterion (f) must consider the reduced test effectiveness shown in Fig. 2 and that this device is not being screened to the same level as parts mounted to boards and tested in pre-unit-level thermal testing. The assessment must determine if previous testing, design margins, and analysis results of the device that will not see pre-unit-level thermal testing can compensate for the reduced test effectiveness shown in Fig. 2.

V. Conclusions

A thermal testing option is provided in MIL-STD-1540E for acceptance electrical and electronic units whereby when pre-unit-level thermal testing satisfies criteria for consistency and completeness, a cycle credit can be taken against unit thermal testing requirements. This option is seen as adding no additional risk to program mission assurance because ESS is accomplished at an earlier level of assembly. Earlier testing typically enables testing to wider temperature ranges with more cycles and higher thermal stresses. Defects found in early testing are easier to repair due to improved access and less schedule constraints. The maximum credit reduces the number of unit-level thermal cycles in half preserving a meaningful unit thermal test program to screen and verify features of the unit that may not have been tested in pre-unit-level thermal tests or that have board-to-board interactions. The biggest risk to this approach is perhaps an inadequate screen at the unit level of devices that were not part of pre-unit-level thermal testing for a variety of reasons. The importance of the assessment of the robustness of these devices cannot be over-emphasized. However, if properly managed, this option is seen as a cost-saving test tailoring approach that reduces the demands of unit-level thermal testing while still meeting ESS requirements.

References

1. "Test Requirement for Launch, Upper-Stage and Space Vehicles," Air Force Command, Space and Missile Center Standard, SMC Standard SMC-S-016, 5 September 2014.

2. Perl, E., Peterson, A. J., Snyder J. M., Wright, C. P. and Welch, J. W., "Test Requirements for Launch, Upper-Stage, and Space Vehicles," Aerospace Report No. TR-RS-2014-00016, 25 June 2014.

3. "Environmental Stress Screening Guidelines for Assemblies," Institute of Environmental Sciences, September 1984.

4. Hamburg, O., and Tosney W., "The Effectiveness of Satellite Environmental Acceptance Tests," The Journal of Environmental Sciences, January/February 1989, pp. 20-26.

5. Quintero, A. H., Welch, J. W., and Wolf, H., "Perceptiveness in Thermal Vacuum Testing," Proceedings of the 18th Aerospace Testing Seminar, March 1999.

6. Gluck, D. F., "Thermal Testing of Space Vehicle Electronic Components," AIAA-86-1302, AIAA/ASME 4th Joint Thermophysics and Heat Transfer Conference, 2-4 June 1986.

7. Welch, J. W., "Lessons Learned in the Application of Thermal Test Requirements for Spacecraft Units," AIAA-2008-4119, 40th AIAA Thermophysics Conference, 23-26 June 2008.

8. Welch, J. W., "Investigation of the Relative Importance of Thermal Test Parameters as Specified in MIL-HDBK-344," 25th Aerospace Testing Seminar, October 2009.

9. Wright, C. P., "Test Effectiveness of SMC-S-016 Unit Thermal Acceptance Testing," 26th Aerospace Testing Seminar, March 2011.