# Electronic Circuit Design and Analysis for Space Applications

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## Abstract
Electronic circuit design and analysis in commercial applications takes into account component parameter variations due to initial tolerance, temperature, and aging. For space applications, the additional component parameter variation due to radiation needs to be taken into account. The charged particles in space radiation environment consist primarily of high-energy electrons, protons, alpha particles and heavy ions (cosmic rays). The radiation effects of these charged particles are dominated by ionization in electronic devices, and the resulting total ionizing dose (TID), single-event effects (SEE), and enhanced low dose rate sensitivity (ELDRS) issues are briefly discussed. Details of circuit design and worst case analysis are presented for two simple circuits: a three-terminal linear regulator, and a relay coil driver. Approaches to the detailed worst case circuit analysis, and an awareness on the need of the analysis to be performed before the design is released to manufacturing should be part of a well-rounded electronics design curriculum.

## Introduction
Electronic circuit design starts with the customer electrical specifications. Environmental specifications such as temperature and life quickly become important design inputs. And for space applications, commercial as well as military, radiation environment becomes a exceedingly important factor in electronics design. Case/junction temperature and TID level for the parts are known only as a best estimate at the start of the electrical design process since mechanical packaging, and thermal and radiation analyses are all carried out in parallel. This situation typically forces the circuit designer to be somewhat conservative in part selection and design approach. In this paper, the space radiation environment is first reviewed briefly including the total ionizing dose, single event effects, and enhanced low dose rate sensitivity of parts. Then the circuit design and analysis is presented in detail for a three-terminal linear regulator circuit and a electromechanical relay driver circuit. These examples are chosen based on their simplicity, however, the design approach and the necessity of detailed circuit analysis is clearly presented. Failure to analyze a circuit design in a timely fashion can cost dearly in terms of cost and schedule due to last minute design changes. The importance of detailed worst-case circuit analysis should be conveyed to the students as part of a well-rounded electronics design curriculum.

## Space Radiation Environment for Electronic Devices
The space radiation environment poses a risk to all earth orbiting satellites and missions to other planets. Charged particles in this environment consist primarily of high-energy electrons,

protons, alpha particles, and heavy ions (cosmic rays). The radiation effects of these charged particles are dominated by ionization in electronic devices and materials. Energy deposited in a material by ionizing radiation is expressed in "rads", with one rad equal to 100 ergs/gram. However, energy loss per unit mass differs from one material to another because of the atomic differences in various materials. For semiconductor devices, the unit of absorbed dose is rads (Si). There are two types of radiation damage induced by charged particle ionization in the natural space environment. These are total ionizing dose [1,2] (TID) and single-event effects [3,4] (SEE). The TID effects are cumulative ionization damage caused by the charged particles passing through a semiconductor device [1,2]. For MOS devices, this ionization traps positive charges in the gate oxide and produces interface states in silicon at the $Si\text{-}SiO_2$ interfaces. These effects cause threshold voltage shifts and decreased channel carrier mobility, resulting in increased leakage current and power supply current, and possible loss of device functionality. For bipolar devices, ionization adversely affects current gain and junction leakage currents, causing significant degradation in device performance. This leads to increased offset voltage and bias current in op-amps and comparators, and loss of accuracy and functionality in analog-to-digital and digital-to-analog converters.

Single event effects [3,4] (SEE) are caused by a high energy single ion (heavy ion or energetic proton) passing through a device. SEE include single event upsets (SEU), single event latchup (SEL), single event burnout (SEB), and single event gate rupture (SEGR). While SEU are non-destructive and do not cause permanent damage to the device, the other single event effects can be destructive. SEU occur due to either the deposition or depletion of charge by a single ion at a circuit node, causing a change of state in the memory cell (bit upset). In very sensitive devices, a single ion hit can cause multiple bit upsets in adjacent memory cells. However, these SEU cause no permanent damage, and sometimes power recycling is all that is needed. Additionally, auto-correcting circuits can be implemented in many designs. SEL can occur in any semiconductor device that has a parasitic n-p-n-p path. A single heavy ion or high-energy proton can initiate regenerative action. This leads to excessive power supply current and loss of device functionality. Device burnout may occur unless the current is limited or the power to the device is recycled. SEL is of most concern in bulk CMOS devices. SEB and SEGR may occur in MOSFETs, however, they are avoidable by design as long as the applied drain and gate voltages are properly derated.

A radiation risk assessment for any electronic device includes the determination of TID and SEE susceptibility of the device caused by the projected radiation environment of the spacecraft. It should be noted that the TID on a device can vary significantly with the amount of shielding interposed between the device and the outside environment, however, the SEE susceptibility do not change significantly with shielding [3,4].

TID testing of devices is generally performed by exposing devices to gamma rays from a Co-60 source with a dose rate of typically 50-300 Rads/sec, per MIL-STD-883. However, dose rates in the natural space environment are very low (0.1 to 10 mRads/sec). It is not feasible to simulate the low dose rate of space environment during ground testing. However, more and more bipolar linear devices such as op-amps, comparators, and linear regulators are tested at low dose rates since the recent discovery of enhance low dose rate sensitivity [5,6] (ELDRS). As a designer,

either we select ELDRS tested parts or design very conservatively especially with input offset voltage and bias currents for linear bipolar ICs.

**Design Examples**

The following two simple examples illustrate the approach to design and analysis as well as the importance of detailed analysis prior to releasing the engineering drawings to manufacturing.

*Three terminal linear regulator*

Consider the three-terminal linear regulator circuit shown in Fig. 1, commonly used to post-regulate the low power outputs of a switching power converter. LT1086 [7], a low dropout linear regulator from Linear Technology is chosen as an example since radiation data on this part is readily available.

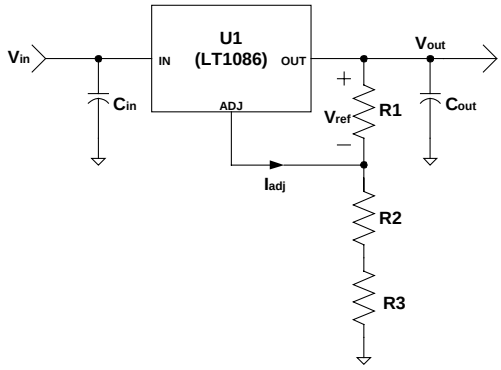


Figure 1 Three-terminal linear regulator circuit.

*Design Requirements:* 10.5 V ≥ Vin ≥ 7.5 V, Vout = 5.0 V ± 5%, and 500 mA ≥ Iload ≥ 100 mA.
*Circuit Design:* Basic design equation can be derived from Fig. 1 as:

$$Vout = Vref \bullet \left(1 + \frac{R2 + R3}{R1}\right) + (R2 + R3) \bullet Iadj \qquad (1)$$

Per the LT1086 datasheet [7] and design requirements, Vref = 1.25 V, Vout = 5.0 V, and Iadj = 55 μA. Selecting R1 as 249 Ω, the required value for (R2 + R3) can be computed using Equation 1 to be 738.9 Ω. The following resistor values will work for this design: R2 = 365 Ω, and R3 = 374 Ω. The power dissipation in the resistors can be computed as $P_{R1}$= 6.25 mW, $P_{R2}$= 9.4 mW, and $P_{R3}$= 9.6 mW. We could easily use 100 mW, 1% thick-film chip resistors of R0805 size with a temperature coefficient of 100 ppm/$^{o}$C. It is possible to get by with 50 mW resistors, however, it all depends on the operating case temperature of the resistors as well as the customer and/or internal parts derating guidelines.

*Worst case circuit analysis:* Let's calculate the worst case steady state dc regulation of the output voltage to see if the design meets the regulation requirement of ± 5%. Variation of component parameters due to initial tolerance, temperature, and space radiation environment needs to be taken into account in the analysis. We are assuming the maximum case/junction temperature to be 85$^{o}$C, a design life of 18 years, and a total dose radiation level of 40 kRads at the part level.

Aging data for resistors can be computed assuming MIL-R-55342 type chip resistors. MIL-HDBK-1547A [8] provides a ±4% degradation at 125°C for 10 years of life. Degradation due to 18 years of life at 85°C can be calculated using Arrhenius aging model given below.

$$Aging\_factor_{85C} = Aging\_factor_{125C} \bullet e^{\left[\frac{E_A}{K}\left(\frac{1}{125+273} - \frac{1}{85+273}\right)\right]} \quad (2)$$

where, K = Boltzman's constant = 8.62e-5 eV/°K, and $E_A$ = activation energy = 1.35 eV (for film resistors).
Based on Equation 2, aging factor is 0.09% at 85°C for 18 years of life.

Next, the initial and temperature variations of Vref and Iadj for LT1086 are obtained from the datasheet [7]. The aging data for these parameters are assumed to be 1%. Finally, the variation of these parameters due to total dose radiation is computed based on available data [9]. The details are shown in Table 1 using the data for Device ID 1086 02 [9].

Table 1 LT1086 Radiation data for Vref and Iadj (Dose rate: 50 Rads/s)

| Vref (Vdiff = 3 V; Iload = 500 mA) | | |
|---|---|---|
| **Device #** | **Initial (V)** | **Delta (mV) at 40 kRads** |
| 2 | 1.25 | -22.9 |
| 3 | 1.24 | -38.7 |
| 4 | 1.25 | -17 |
| 5 | 1.24 | -22.3 |
| 9 | 1.24 | -31.2 |
| 12 | 1.25 | -23.4 |
| 13 | 1.24 | -27.7 |
| 15 | 1.24 | -24.1 |
| Average | 1.24375 | -25.9125 |
| Std Dev | | 6.60982764 |
| Avg+3*std dev | | -6.0830171 |
| Avg-3*std dev | | -45.741983 |
| Max variation (mV) | | -45.741983 |
| **Max variation (%)** | | **-3.6777474** |

| Iadj (Vdiff = 3 V, Iload = 10 mA) | | |
|---|---|---|
| **Device #** | **Initial (uA)** | **Delta (uA) at 40 kRads** |
| 2 | 8.3 | 0.505 |
| 3 | 8.3 | 0.505 |
| 4 | 8.3 | 0.505 |
| 5 | 8.3 | 0.505 |
| 9 | 8.3 | 0.505 |
| 12 | 8.3 | 0.505 |
| 13 | 8.3 | 0.505 |
| 15 | 8.3 | 0.505 |
| Average | 8.3 | 0.505 |
| Std Dev | | 0 |
| Avg+3*std dev | | 0.505 |
| Avg-3*std dev | | 0.505 |
| Max variation (uA) | | 0.505 |
| **Max variation (%)** | | **6.08433735** |

Table 2 below provides a summary of part degradation data for the linear regulator design.

Table 2 Part degradation database for three-terminal linear regulator

| Ref Des. | Parameter | Nom. Value | 25C Max Value | 25C Min Value | Max Temp (deg C) | Min Temp (deg C) | Temp Coeff. | Temp Coeff. Type | Aging Max (%) | Aging Min (%) | RADIATION Value | RADIATION Rad Level | DESIGN Max Limit | DESIGN Min Limit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R1 | Resistance (Ω) | 249 | 251.49 | 246.51 | 85 | -35 | 0.01 | Linear (%/°C) | 0.08869 | 0.0887 | 0 | | 253.20485 | 244.79515 |
| R2 | Resistance (Ω) | 365 | 368.65 | 361.35 | 85 | -35 | 0.01 | Linear (%/°C) | 0.08869 | 0.0887 | 0 | | 371.16374 | 358.83626 |
| R3 | Resistance (Ω) | 374 | 377.74 | 370.26 | 85 | -35 | 0.01 | Linear (%/°C) | 0.08869 | 0.0887 | 0 | | 380.31572 | 367.68428 |
| U1 | Vref (V) | 1.25 | 1.275 | 1.225 | 85 | -35 | 0 | Linear (%/°C) | 1 | -1 | -0.0463 | 40 kRads | 1.2875 | 1.16625 |
| | Iadj (uA) | 55 | 82.5 | 30.525 | 85 | -35 | 18.2 | Linear (%/°C) | 1 | 0 | 3.355 | 40 kRads | 96.415 | 20.515 |

Now we can calculate the worst case upper and lower bound of the output voltage using the following equations.

$$Vout,\max = Vref,\max \bullet \left(1 + \frac{R2,\max + R3,\max}{R1,\min}\right) + (R2,\max + R3,\max) \bullet Iadj,\max \quad (3)$$

$$Vout,\min = Vref,\min \bullet \left(1 + \frac{R2,\min + R3,\min}{R1,\max}\right) + (R2,\min + R3,\min) \bullet Iadj,\min \quad (4)$$

Using the appropriate values from Table 2, Vout,max and Vout,min are calculated to be 5.31 V and 4.58 V, respectively. The required range is: 5.25 V ≥ Vout ≥ 4.75 V. Therefore, the design does not meet the ±5% regulation requirement over the desired temperature, life, and radiation conditions. What options do we have in improving the dc regulation of the output voltage ? We could potentially use 0.1% tolerance resistors with 50 ppm/$^{o}$C temperature coefficient. If that does not help much, only other thing we could do is to use a better linear regulator with a much tighter Vref and Iadj. As an example, we could use RH1086, the much more expensive radiation hardened version of LT1086.

This example shows how important it is to pick the right components when we are designing to a tight specification, and how a detailed analysis can help us in selecting the right part. Additionally, the radiation data on LT1086 was obtained at a dose rate of 50 Rads/s. The dose rate typically seen by parts under natural space radiation is in the neighborhood of 5-10 mRads/s. And this low dose rate makes the variation of Vref and Iadj even worse resulting in a output voltage dc regulation poorer than the above estimate. Low dose rate data on RH1086 is available[9] at a dose rate of 100 mRads/s. This data suggests that it will be hard to achieve a ±5% dc regulation. Choices we might explore are: (1) negotiate with the customer to see ±5% is a real requirement or they can live with, e.g., ±7%, (2) look for a better rad-hard low dropout linear regulator, and (3) if all else fails, design a discrete linear regulator with a much tighter reference.

*Electromechanical relay coil driver*

Next, we will consider a simple relay coil driver circuit shown in Fig. 2. The control voltage is typically a TTL/CMOS type digital logic output. Any time the control voltage is high, Q2 is turned on thereby forward biasing Q1. Once Q1 turns on, the input voltage, e.g., 28VDC, is connected to the relay coil. As soon as the control voltage goes to zero, Q2 turns off thereby turning off Q1. Thus the input dc voltage is disconnected from the relay coil, and the energy trapped in the coil is dissipated in the coil resistance through the freewheeling diode D1.

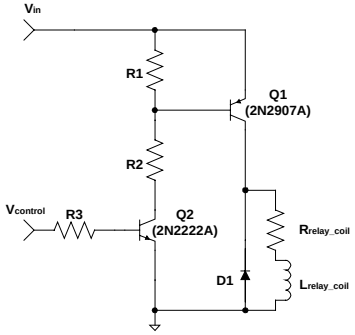


Figure 2 Electromechanical relay coil driver circuit.

*Design requirements:* 35V ≥ Vin ≥ 25V, Icoil,max = 150 mA, and Vcmd,high (MIN) = 4 V.
*Circuit Design:* Assuming a minimum dc current gain of 50 for Q1 at 150 mA of collector current, the required maximum base current is 3 mA. When Q1 and Q2 are on, voltage across R1 is 0.7 V. Assuming a Vce,sat of 0.3 V for Q2, minimum voltage across R2 is 24 V and maximum current through R2 is 3.07 mA. Therefore, R2 needs to be 7.82 kΩ (=24 V/3.07 mA). We can use a R2 of 7.68 kΩ. This corresponds to a maximum Q2 collector current of 4.4 mA (=34 V/7.68 kΩ). Now, assuming a minimum dc current gain of 25 for Q2, R3 can be calculated to be 18.7 kΩ (=25∗(4–0.7) V/4.4 mA)).
*Worst case circuit analysis:* Since radiation level and operating temperature have significant effects on the bipolar transistor's dc current gain, we will first estimate the worst case end-of-life (EOL) current gain of Q2 (2N2222A) assuming a maximum junction temperature of 85°C, a minimum junction temperature of –35°C, total dose radiation of 75 kRads at the part level, and a design life of 18 years. Our design assumed this worst case gain to be 25. Degradation due to radiation effects can be calculated using the following equation.

$$h_{FE,post\_rad} = \frac{1}{\frac{1}{h_{FE,pre\_rad}} + \Delta\left(\frac{1}{h_{FE}}\right)} \tag{5}$$

where,

$$\Delta\left(\frac{1}{h_{FE}}\right) = \frac{1}{h_{FE,post\_rad}} - \frac{1}{h_{FE,pre\_rad}} \tag{6}$$

Based on 2N2222A radiation data [9] (Device ID = 2N2222A 68) for Ic = 1 mA and Vce = 10V, $h_{FE,post\_rad}$ is computed to be 39.1. Details of the calculation are shown in Table 3.

Table 3 Calculating the post-radiation dc current gain of 2N2222A

| Device # | Initial | 75 kRads | Delta (1/hFE) |
|---|---|---|---|
| 78 | 166 | 62.6 | 0.009950345 |
| 81 | 212 | 68.5 | 0.009881559 |
| 82 | 242 | 76.4 | 0.008956774 |
| 83 | 262 | 75.7 | 0.009393246 |
| 85 | 236 | 70.7 | 0.009906983 |
| 87 | 222 | 68 | 0.010201378 |
| 88 | 219 | 70.8 | 0.009558084 |
| 90 | 207 | 73.6 | 0.008756039 |
| 91 | 184 | 59.5 | 0.01137194 |
| 92 | 171 | 66.3 | 0.009235003 |
| 93 | 222 | 81.8 | 0.007720434 |
| 94 | 186 | 71.7 | 0.008570657 |
| Mean | 210.75 | 70.46666667 | 0.009458537 |
| StdDev | 29.36951109 | 6.120061398 | 0.000927048 |
| Mean+3 Sigma | 298.8585333 | 88.82685086 | 0.01223968 |
| Mean-3 Sigma | 122.6414667 | 52.10648247 | 0.006677394 |
| Minimum initial | | 75 (From MILSPEC data at 1mA) | |
| HFE post-rad | 39.10372205 | | |

Now, the temperature and aging degradations are to be accounted for. Temperature coefficient for dc current gain can be defined as:

$$TC = 1 - \left( \frac{h_{FE,-55C}}{h_{FE,25C}} \right)^{\frac{1}{25-(-55)}} \tag{7}$$

Using 2N2222A datasheet [10], *TC* is calculated to be 0.008761 for a collector current of 1 mA. Degradation due to aging is assumed to be 25% per MIL-HDBK-1547A [8] at 105°C for a life of 10 years. For a junction temperature of 85°C, the aging degradation can be obtained using the Arrhenius equation given below:

$$Aging\_factor_{85C} = Aging\_factor_{105C} \bullet e^{\left[ \frac{E_A}{K} \left( \frac{1}{105+273} - \frac{1}{85+273} \right) \right]} \tag{8}$$

where, K = Boltzman's constant = 8.62e-5 eV/°K, and $E_A$ = activation energy = 1.1 eV (for semiconductors).

Based on Equation 8, degradation due to aging at 85°C is computed to be 3.8%. This corresponds to an aging degradation of 6.84% for 18 years of life. Now, the worst case EOL dc gain can be computed using:

$$h_{FE,EOL} = h_{FE,post\_rad} \bullet (1 - TC)^{25-(-35)} \bullet (1 - Aging\_factor) \tag{9}$$

The worst-case dc current gain for 2N2222A at 1 mA of collector current is computed to be 21.5 using Equation 9. Therefore, the design assumption of a minimum gain of 25 is not correct for the specified temperature, life, and radiation environment. What options do we have as a designer ? We can always design for higher Q2 base current by reducing R3. The lesson here is we better perform detailed circuit analysis before the circuit board layout is released, and thereby avoid the initiation of a series of engineering change notices after manufacturing starts.

We can perform a similar analysis for Q1 (2N2907A) to see if the assumed worst case gain of 50 at 150 mA of collector current is justifiable. Radiation data on this part is readily available [9]. If the worst case device gain turns out to be less than 50, we can decrease R2 to provide for additional base current. However, this will increase the collector current of Q2, and may require readjusting R3.

**Summary**

The space radiation environment as it relates to electronic circuit design is presented. The total ionizing dose, single event effects, and enhanced low dose rate sensitivity in linear bipolar integrated circuits are discussed. Two simple examples illustrated the design process and the worst case circuit analysis that considers the environmental requirements such as temperature range, life, and radiation environment. The chosen example circuits are not prone to single event effects. However, for analog circuits based on op-amps, comparator, and pulse width modulation ICs, as well as most digital circuits are susceptible to single event effects. This will require estimation of upset rate [3] as well as upset mitigation schemes. The importance of and

approaches to worst-case circuit analysis should be made part of a well-rounded electronics curriculum.

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